

**CIRCUIT
INSTRUCTION
MANUAL**

PDP-6

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MANUAL**

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PDP-6 CIRCUITS

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PDP-6 CIRCUITS

CHAPTER 1 INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION AND SCOPE

The purpose of this instruction manual is to aid personnel in maintenance, at the circuit level, of the DEC Programmed Data Processor-6. The manual contains complete descriptions of all circuits found in the Type 166 Arithmetic Processor, Type 162 Fast Memory, and in the control logic for four peripheral devices usually included in the installation: Type 760 Paper Tape Reader, Type 761 Paper Tape Punch, Type 626 Teletype Printer-Keyboard, and Type 461 Card Reader. Also included are all standard logic circuits used in the interfaces and control portions of Core Memories Types 161C and 163C; all special circuits associated with a core stack, such as the regulated power supply, core drivers, switching circuits, and sense amplifier, are described in the maintenance manual for the memory in which they are used. Troubleshooting information is included as it pertains to module replacement and repair; detailed information on system operation and troubleshooting may be found in the maintenance manuals for the PDP-6 arithmetic processor and memory. Descriptions of circuits unique to any equipment not listed above are included in the appropriate maintenance manuals.

Where possible, material common to circuits in a given class, such as basic inverter or flip-flop operation, supply voltages, and common jumper codes, is presented in the introductory remarks for each chapter. Timing characteristics common to each of the three DEC module series (1000, 4000, 6000) are also included here. The remainder of each chapter consists of material applicable to individual circuit types, such as circuit logic (if required), connector information, unique jumper codes, and all special circuitry.

Schematic diagrams for all circuits, with modified logic diagrams of a few complex modules, are grouped at the rear of the manual in order by type number. No figure references are made in individual unit descriptions, but references to applicable schematics are implied.

1.2 PDP-6 MODULES

The DEC Programmed Data Processor-6 is constructed of digital modules and power circuits. The module components are mounted on a dip-soldered epoxy board surrounded by an aluminum frame measuring (with some exceptions) $1/2 \times 4-1/2 \times 7$ inches. Logic and power connections are made through 22-pin Amphenol plugs, connected to the circuits by flexible wiring to minimize strain.

DEC circuits can be categorized by function and by maximum operating frequency. PDP-6 circuits fall into seven functional groups:

PDP-6 CIRCUITS

Inverters
Diode gates and decoders
Flip-flops
Amplifiers
Delays
Pulse circuits
Power circuits

Most types are discussed in some detail; however, the first two groups (simple inverter and diode networks) are described collectively, since the reader is assumed familiar with basic solid state electronics.

A DEC module (any circuit in the first six classes) is assigned one of three maximum operating frequencies, 500 kc, 5 mc, or 10 mc---the 4000, 1000, and 6000 series respectively (although some 4000 series modules can operate at 1 mc). Module timing characteristics are commensurate with these speed categories. DEC standard pulse widths are 0.4 μ sec for the 4000 series, 70 nsec for the 1000 series, and 40 nsec for the 6000 series. These pulses are 2.5v in amplitude. Tolerances are +2.3 to +3.0v and -2.3 to -3.5v. DEC signal levels are standard for all modules at ground and -3v. Tolerances are 0 to -0.3v and -2.5 to -3.5v.

To facilitate system wiring, four connector pins on each module are reserved for supply voltages: two pins, A and B, carry +10 vdc (for ease in submodular marginal checking), pin C supplies -15 vdc and pin D is grounded. Additional pins may be used for ground as necessary. All modules that require it have a built-in source of -3 vdc, which utilizes the 0.75v forward drop of the silicon diode. Four series diodes are used, biased to -15 vdc, usually through 560 ohms (figure 1-1). The resistor accepts enough current to regulate the supply under all load conditions.

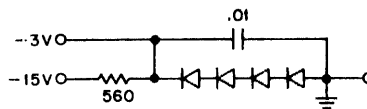


Figure 1-1 Standard -3 vdc Supply

Five PDP-6 modules, Flip-Flops 1250 and 6205, and Amplifiers 1664, 1665, and 6615, require special consideration. These types have three times the area of the standard DEC module and are serviced by two DEC mounting panels at each end--a packaging technique that permits a considerable reduction in space, in module types, and in external connections when the number of repetitive, interdependent circuits is large. Each pin designation on these five schematics is therefore two letters, the first indicating the connector (A, upper front; B, lower front; R, upper rear; S, lower rear), the second referencing a single pin of the selected connector. (On logic diagrams of the PDP-6 computer, letter designations of the

appropriate mounting panels replace the front connector prefixes; rear prefixes remain the same.) Two other modules, Flip-Flops 6203 and 6206, are double-length, standard-height types and are serviced by single connectors at both ends. Rear connectors have the usual R prefix.

A number of modules have provision for internal jumpering, which permits their use in a variety of applications without requiring additional external connections. Positions at which jumpers can be used are indicated on the schematics by dotted lines between unlettered terminals. Spare modules are delivered with all jumpers in place, and the technician must cut out the ones not wanted. On the UMLs, the type numbers for jumperable modules are followed by number or letter combinations that indicate jumper configurations (all such connections are shown on the logic drawings). Decoding methods for these symbols are given with the module descriptions.

On some circuit schematics, certain groups of passive components have a type number but no value designations; these are encapsulated elements whose values are called out elsewhere on the schematic. They appear on the modules as rectangular orange capsules.

PDP-6 modules containing only clamped loads, terminating resistors, or indicator lamps are considered self-explanatory and are not discussed here, although their schematics are included at the rear of the manual.

Replacement schematics for the circuits have drawing numbers of the form RS-X-N, where X is a letter indicating drawing size and N is the circuit type number, usually three or four digits. To the right of the drawing number is another, the revision number of the circuit schematic. To the left is a letter that indicates the revision of the circuit board. The revision letter is etched on the board and printed after the type number on the aluminum frame of the module.

1.3 PERTINENT DOCUMENTS

The following documents augment these discussions presented in this book.

- a. System Modules Catalog, C-100
- b. PDP-6 Arithmetic Processor 7F-67 (166)
- c. PDP-6 Fast Memory Type 1621 Core Memory Type 161C, F-67 (162-161C)
- d. PDP-6 Fast Memory Type 1621 Core Memory Type 163C, F-67 (162-163C)

Within this text constant reference is made to standard modules and configurations. All module information such as detailed circuit schematics can be found in the module catalog. References to PDP-6 applications of decoders, etc., can be further studied in the PDP-6 Arithmetic Processor 166 Manual.

CHAPTER 2

INVERTERS AND GATES

Most logical operations in the PDP-6 are performed with saturating inverters and diode gates. Because of their relatively simple design and because of the consistent use of inverters as gate buffer amplifiers, both groups are described in this chapter. For information on number of circuits per module, pin connections, jumpers, etc, refer to the DEC System Module Catalog, C-100. Many of these modules have clamped loads that do not appear at the output connectors but may be jumpered internally to inverter collectors. The presence of a jumper is indicated by a 1 in a jumper code of n bits (octal), where n is the number of clamped loads in the module. From left to right the bits correspond to the alphabetical order of the collector pins at the connector. An R is used in place of a number to indicate that all clamped loads are connected.

2.1 INVERTERS

An inverter can be used as a level gate or a pulse gate. Inverter transistors are pnp type, and operate either in saturation or in cutoff. The collector-emitter impedance of a saturated transistor is very low; at cutoff, it is very high. If the emitter is grounded and the collector is connected to a negative load, the collector output is inverted with respect to the base input. Base input loading is supplied by the 3K resistor (figure 2-1); a saturating base current of 1 ma therefore flows through the transistor when -3 vdc is present at the input. A bypass capacitor at the input provides overdriving current which speeds switching. The more positive input to an inverter usually is derived from the collector of a saturated transistor (approximately -0.2 v). Base bias at 0 vdc (input unterminated) is supplied by a divider between $+10$ and -15 vdc. This allows marginal checking inverter base leakage (simultaneously checking collector saturation voltage of the stage preceding the inverter) and inverter dc gain.

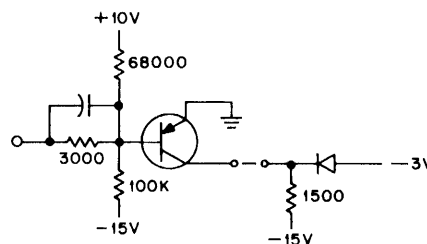


Figure 2-1 Standard Inverter

The diode in the clamped load limits the negative voltage at the inverter output, supplying the current needed to maintain the output at -3v . With a 1.5K load resistor, diode current is a maximum of 8 ma under no-load conditions and decreases to 0 as the current drawn from the external load increases to 8 ma .

Delay through a 4000-series inverter is 300 nsec (defined as the time between the point of 10% input change and 10% output change); the 1000-series delay is 20 nsec , whereas that of a 6000-series inverter is approximately 12 nsec .

2.2 GATES

The PDP-6 diode modules are of three basic types: simple networks for general purpose pulse and level gating; capacitor-diode gates; and decoders.

2.2.1 Diodes

The diode gate modules contain two or more diode logic gates, consisting of a number of diode-coupled inputs driving an inverter base. A clamped load is available for each inverter. The gating diodes provide either the AND or the OR function for a given assertion level; the transistor amplifies and inverts the diode output so that the diode-inverter combination is properly termed a NAND or NOR gate. In the negative NAND gate shown in figure 2-2, Q1 is driven into conduction only if A, B, and C are all negative (-3 vdc), allowing R1 to forward-bias the transistor emitter-base junction. With ground at any input, R2 reverse-biases the junction and cuts off the transistor.

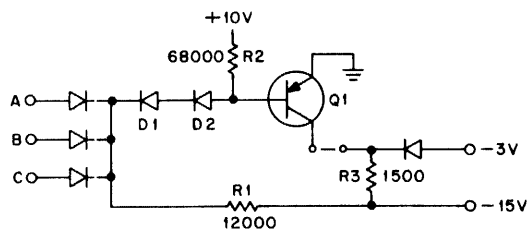


Figure 2-2 Negative Diode NAND Gate

If the source of a nominal ground input is the collector of a saturated transistor, the actual input voltage is slightly negative. The drop across the gate diodes further reduces the voltage applied to the inverter. To compensate for these reductions in input ground levels, two series silicon diodes, D1 and D2, are employed as level shifters between the gate proper and the inverter base. The shift is large enough to ensure positive bias at the base and hence reliable cutoff when any normal ground input is applied to the gate.

The negative diode NOR gate shown in figure 2-3 drives Q2 into saturation through input resistor R4 when -3 vdc is applied to D, E, or F. When none of the inputs are negative, R5 cuts off Q2 by reverse-biasing the emitter-base junction. A diode, D3, is always placed across this junction to prevent the transistor base from being driven too positive when no input connections are made. R5 may actually be two resistors connected to both +10v supplies, as is done in module 6116. This prevents undue sensitivity of the circuit to marginal voltages.

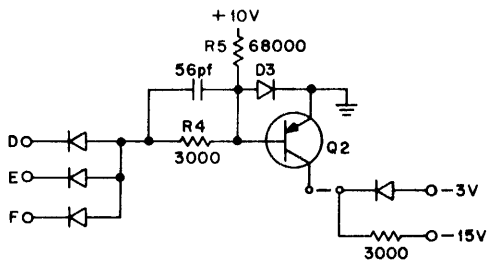


Figure 2-3 Negative Diode NOR Gate

2.2.2 Capacitor-Diode Gates

In the basic positive capacitor-diode gate shown in figure 2-4, a positive pulse or level change at A produces a positive pulse at C, provided a ground enabling level has been present at B for a certain interval before the pulse. This interval depends on the resistor-capacitor time constant, and is the time required for the common junction voltage to rise sufficiently close to ground. The gate is inhibited when the junction voltage falls close enough to -3 vdc that the input pulse cannot forward bias the diode. A clamped load often connects to the gating level input. In the basic negative gate the diode polarity is reversed, and the pulse input, enabling input, and output are negative. A complete capacitor-diode circuit provides pulse amplification in an inverter, which is associated with a single gate or shared among several. In all positive gate modules the inverter is at the pulse input; in all negative modules, at the pulse output. Thus, regardless of the polarity of the gating level, all modules accept a negative pulse or level change and produce a positive-going output.

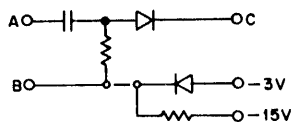


Figure 2-4 Basic Positive Capacitor-Diode Gate

The circuit at the left in the 4127 schematic is typical of negative capacitor-diode gates. A -3 vdc level applied to F enables the gate; a negative pulse or level change at E then generates a positive-going output pulse at H. The delay inherent in this circuit requires that the gating level be present at least $1 \mu\text{sec}$ before arrival of the pulse. When F becomes negative, the C1-D1 junction falls from ground to -3v , the fall time being determined by the time constant of C1-C2. After this interval, a negative pulse applied to E is sufficient to forward-bias D1 and pass through the diode to the load. The gate output is referenced by R5 to a dc level of -3v . D2 and R1 prevent the gate input from going more negative than -3v , preventing undue sensitivity of the circuit to noise at E. When D1 is forward-biased by a pulse at E, the negative pulse at the D1-R5 junction is coupled through C2 to the Q1 base. As the transistor turns on, output H rises to ground. At the trailing edge of the input pulse, D1 is cut off. The Q1 base is normally biased positive by R3-D3 to reduce noise susceptibility.

The circuit in the upper left of the 4128 schematic is typical of positive capacitor-diode gates. The pulse input P can be driven by a standard negative pulse or by a negative-going level change with a maximum fall time of $5 \mu\text{sec}$. Each gate is enabled by a ground level that must be present at least $1.5 \mu\text{sec}$ before arrival of the pulse; however, for a transfer of 1s or 0s only, all off gates must be disabled for $4.5 \mu\text{sec}$ before readin. If the D2 cathode is tied to the base of a saturated transistor, it is near ground potential. A -3v to ground pulse or level change at the Q1 collector is coupled through C4 but can forward-bias D2 only in the presence of a ground level at F.

2.2.3 Decoders

The decoder modules contain special diode configurations that decode a given binary information group to an assertion at one of several possible outputs. The Type 1151 contains an 8-section diode matrix that is driven by the 1 and 0 outputs of three flip-flops. Each section is a 3-diode negative AND gate, which receives a unique combination of inputs representing one of the eight states of the three flip-flops. The assertion of a specific binary input configuration thus turns on a single output inverter. For example, when all flip-flops are 0, the output of the gate at the far left of the schematic, whose inputs are connected to the flip-flop 0 outputs, is at -3 vdc. The outputs of all other diode gates are at ground. At any time, therefore, all inverter outputs are negative except the one driven by the satisfied diode gate. The entire module can be gated on or off at the common emitter connection of the inverters, or the emitters can be jumpered to ground internally or grounded at the connector.

Types 4151 and 6151 are identical to the 1151 in all respects except speed. The 6150 is similar to the 6151 except for inverted logical sense (all inputs to a gate must be at ground to obtain a unique negative decoder output), internally grounded emitters, and a common enable input to the diode matrix.

The Type 6155 contains two binary-to-quarternary networks. Each output inverter is driven by a 3-input diode AND gate, which is in turn driven by the outputs of two flip-flops and a common enabling level. When all three inputs to a given gate are negative, the ground output of its associated inverter is uniquely asserted.

2.3 MAJORITY LOGIC

In the memory protection and relocation networks are two circuits that employ majority logic. Type 6131 is a dc adder which uses majority logic to develop the carry output; Type 6132 contains two majority gates which form part of the borrow chain in an arithmetic comparison.

In addition there must be a carry to the next more significant bit if two or more of the three inputs (two summands and a carry) are 1s. For subtraction, the minuend bit is complemented, and the carry output then represents a borrow to the next bit. If inverter or diode gates were used to develop the carry output, separate AND gates to decode all four possible input cases that necessitate a carry would be necessary, as well as an OR gate to form the output. Majority logic does not differentiate as to the source of the logic inputs; instead, all three are fed to precision resistors and the voltage at the junction point is compared to a fixed threshold by a difference amplifier. The summing resistors are paralleled by speed-up capacitors and the two-stage difference amplifier used in both modules operates far from saturation. Consequently the propagation delay for the carry is less than 10 nsec per bit.

2.3.1 6132 Majority Gate

This module consists of two gate circuits and appropriate internal supply voltages. The output of a gate is asserted whenever at least two of its three inputs are asserted. In the protection logic the A input (pins X and E respectively of the left and right gates) is an MA bit on 1, the B input is a PR bit on 0. These inputs are labeled \bar{A} IN and \bar{B} IN because they are made through inverters and hence require opposite assertion to C IN, which is the carry from the next less significant stage. The carry out is available at both polarities. Since these circuits are used in series, the carry output of the left gate is wired internally as the carry input to the other but is available at the connector via an internal jumper. If the A and B inputs to a series of gates represent 1s in a pair of numbers, C is the carry function. If one set of inputs, e.g., B, represents 0s, C is the borrow function of B-A.

The A and B inputs have ground assertion and drive standard DEC 6000-series inverters with clamped loads (for example Q1-Q4 in the left gate). The three majority logic resistors (R3-R6-R9) are tied together at the left base of Q2, the first stage of the difference amplifier. The carry input is asserted negative at R3 to correspond logically with the inverted signals at R6 and R9. The two emitters of Q2 are tied together to R8, a current sink to -15 vdc. When two or more of the inputs to the resistance summing

network are $-3v$, the sum point (left base of Q2) falls below $-1.5v$, cutting off the left side of Q2 and allowing the right side to conduct all current. Conversely when two or more inputs are at ground, the summing point rises above $-1.5v$ turning on the left side and cutting off the right. Neither Q2 collector can saturate however because current sink R8 conducts a maximum of 1.5 ma which cannot bring either collector below ground.

The difference amplifier output stage is Q3 whose bases are driven directly by the Q2 collectors. The emitter current source for Q3 is R4 to +10 vdc; the collectors are clamped to 0 and -3 vdc by D2 and D3 on the left, D4 and D6 on the right. Coils L1 and L2 provide shunt inductive frequency compensation for the Q2 collectors to enhance propagation speed. C4 and C8 as well as the various capacitors associated with the series voltage supply at the right serve to keep voltage supply points free from transients.

2.3.2 6131 DC Adder

This module contains a majority gate, an exclusive OR network, and supplies for the necessary internal voltages. If bits from two summands are asserted ground at pins E and F, and a carry in is asserted ground at L, negative at T, a bit of the sum appears at outputs X and Y (ground and negative, respectively) and the carry out to the next more significant stage appears in both polarities at U and K. The negative sum out is also available at pin W isolated through a resistor to drive an indicator. A fifth input, pin H, receives a ground enable level. When the enable falls to -3 vdc, the F input is negated internally and consequently the sum output is identical to the E input (assuming there is no carry in, which would ordinarily be the case). In the computer, these circuits relocate memory addresses for the user mode. For this application input E receives an MA bit, F an RLR bit, the carry inputs come from the next less significant adder, and H receives the relocate enable level from executive mode control.

In the schematic the inverters for inputs E, F, and H are at the top left. Below these are two exclusive OR stages and an output current switch (difference amplifier). To the right of center is a difference amplifier for the majority gate and at the far right is the series-diode voltage source. Except for the input inverters and common internal supply, the sum and carry networks are completely independent. Inputs E and F drive Q2 and Q6, the latter paralleled by Q8 so that a negative level at H prevents negative assertion of the F input at the Q6 collector. Both inverter loads are clamped at -3 vdc by D1 and D2. L is the carry input of the majority gate, whose input for the adder is T.

The adder uses two exclusive OR stages to produce a sum in the same way as do the arithmetic register bits except that the output depends only on the propagation of level changes rather than pulsed flip-flop changes. The first stage produces a partial sum from the two summand inputs; the second stage then inverts this partial sum whenever there is a carry. In other words when neither or both summands are asserted, the sum output is equal to the carry input; otherwise the sum is the inversion of the carry. The first stage consists of transistors Q3 and Q5 with associated RC base feeds. The Q3 and Q5 collectors are

tied together so that the output at the D3 clamp can be $-3v$ only when both are cut off. In this exclusive OR pair, the base of one transistor is driven through an RC network from the emitter of the other. Consequently when both emitters are at the same voltage both transistors are cut off; only when the two emitter drive signals differ can one of the pair saturate. The collectors are at $-3v$ whenever the E and F inputs are identical, at ground when they differ.

The second exclusive OR stage is Q1 and Q7 with similar cross connection from emitters to bases. The first stage drives the Q1 emitter through an RC network; the emitter of Q7 receives the carry, asserted ground at T, through a similar RC net. When E and F are identical, the Q7 base is $-3v$ so Q7 conducts whenever there is a carry. When E and F differ, the Q7 base is at ground and Q1 determines the sum as the complement of the carry. In order to prevent saturation in this stage the Q1-Q7 collector junction is not clamped at -3 vdc; only the input inverters and the first exclusive OR stage can saturate. Since emitter current sources R2 and R16 cannot allow current sufficient to bring the second-stage collectors more positive than $-3v$, saturation does not occur. The Q1-Q7 collector junction drives the left base of Q4, but the right base is held at $-4.5v$ from the series-diode voltage source at the far right. When either Q1 or Q7 conducts, the left half of Q4 supplies all the current through R14 to $-15v$, pulling the sum 1 output, pin Y, down to the $-3v$ clamp level. The right collector of Q4 floats, clamped at ground by D7, thus negating the sum 0 output at pin X. When Q1 and Q7 are both cut off, the right half of Q4 brings the X output negative, whereas the floating left collector allows Y to return to the ground clamp level.

Input inverters Q2 and Q6 also drive R11 and R10, two of the three majority logic input resistors. The third resistor R17 is driven directly by the negative carry input at pin L. The junction point of the three resistors drives the left base of Q9, the first of two difference amplifier stages that develop the carry output. The Q9 emitters are paralleled; current sink R23 accepts enough current to drive Q10 but not enough to saturate Q9. The right base of Q9 is held at $-1.5v$ from the diode voltage supply. The difference amplifier formed by Q9 and Q10 is identical to that in the majority gate discussed in the preceding section. It develops the carry output at pin K (at the left Q10 collector), clamped at 0 and -3 vdc by D10 and D9. The complement is available at pin U from the right collector, clamped by D11 and D12.

CHAPTER 3 FLIP-FLOPS

Of the flip-flop types used in PDP-6, the 1260, 4706, 4707, 6203, 6205, and 6206 perform rather complex logical operations, so modified logic diagrams for these modules have been included with the schematics to make circuit identification and component location easier. In many flip-flop modules, jumpers select the outputs that appear at the connector or select the flip-flop states produced by a preset pulse. In either case the side of a flip-flop to which a jumper is connected is indicated by a bit in a jumper code of n bits (octal), where n is the number of jumperable flip-flops in the module. The bits left to right correspond to the alphabetical order of the flip-flop outputs at the connector. Other codes unique to particular modules are given in the module descriptions.

The flip-flop, or bistable multivibrator, is a two-state device used primarily for short term storage. A simple flip-flop can be constructed by interconnecting two grounded-emitter inverters (figure 3-1). When one inverter is cut off, its output is negative; this holds the other transistor on, which in turn holds the first transistor off. The state of the flip-flop can be changed by driving either the base of the conducting transistor or the collector of the nonconducting one with a positive-going pulse (although the latter method requires a more powerful driving source). It is this ability of the flip-flop to remain in the state to which it is driven, even after removal of the activating signal, which permits its use as a storage device.

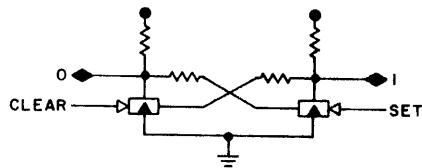


Figure 3-1 Basic Flip-Flop

It is often desirable to reduce flip-flop output impedance in order to drive heavier loads. For this reason, many flip-flop modules are equipped with buffer inverter or emitter follower amplifiers at the outputs. Delay networks are used in PDP-6 flip-flops when speed considerations prevent the use of capacitor-diode gates and intrinsic circuit delay is not sufficient to allow output terminals to be sensed while input terminals are being pulsed.

3.1 OPERATION OF COMPONENT CIRCUITS

To avoid repetition, six circuits basic to the operation of many PDP-6 flip-flops are discussed in this section. Although component values may differ in some instances when the same circuit is represented in several speed lines, the descriptions of these circuits are not dependent on operating frequency.

3.1.1 Unbuffered Flip-Flop

Figure 3-2 shows this circuit, with a type of input gating commonly used with 4000-series flip-flops, the positive capacitor-diode gate. The flip-flop is stable in either of two states: Q1 conducting and Q2 cut off, or vice versa. Its state can be changed by applying a positive-going pulse to the base of the conducting transistor or to the collector of the nonconducting transistor.

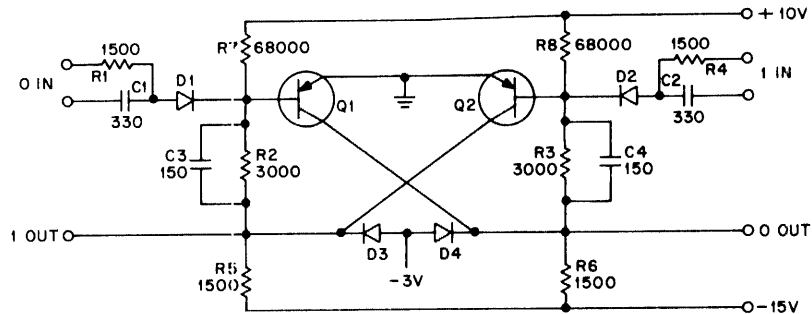


Figure 3-2 Unbuffered Flip-Flop with Positive Capacitor-Diode Input

Since the collectors of Q1 and Q2 are resistively cross-connected to the opposite bases, R2 and R3 hold the flip-flop in its new state after the disappearance of the trigger pulse. Base bypass capacitors C3 and C4 provide overdriving current to the transistors to speed switching. The flip-flop is said to be in the 0 state when the 0 output terminal is quiescent at -3 vdc and the 1 output is grounded. Q2 remains saturated and Q1 cut off until the flip-flop is set through capacitor-diode gate D2-C2-R4. This gate is enabled by a ground level at the R4 input, raising the D2-C2 junction to ground. A standard positive voltage step applied to the C2 input then forward-biases D2 (if a ground enable is present at R4) and turns off Q2. The sharp negative spike caused by the differentiation of the pulse trailing edge is discharged through R4.

As the positive-going trigger reverse-biases Q2, the resulting negative transition at its collector is coupled through the parallel combination of R2 and C3 to the Q1 base. As this point falls below the Q1 emitter, Q1 conducts and its collector rises to ground. This level is, in turn, coupled through C4 and R3 back to the Q2 base, allowing R8 to maintain Q2 at cutoff. The flip-flop is now in the 1 state. D3-R5 and D4-R6 are output clamped loads. The flip-flop is cleared back to 0 by enabling the C1-R1-D1 gate and applying a positive pulse to the Q1 base. Unbuffered flip-flop delay is approximately 50 nsec, 25 nsec, and 12 nsec for the 4000, 1000, and 6000 series, respectively.

3.1.2 NPN Emitter Follower

The npn emitter follower, shown in figure 3-3, with clamped loads at input and output, is often used as an auxiliary amplifier for positive-going set and clear trigger pulses where no signal inversion is desired. Its output impedance is low for positive-going pulses or level changes; current is supplied to the load by the transistor rather than by a load resistor.

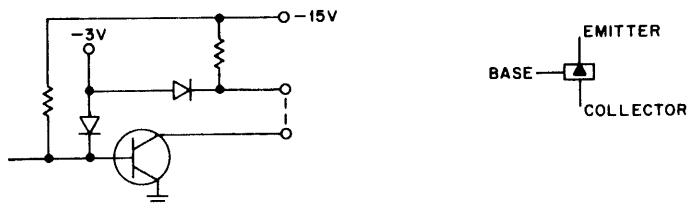


Figure 3-3 NPN Emitter Follower

Since, as a current amplifier, the npn emitter follower can operate with less drain on external trigger circuits than would a diode-clamped load configuration, it permits the use of remote trigger sources that may require long transmission lines and terminating resistors.

3.1.3 Flip-Flop with Output Buffers

Addition of output buffer amplifiers to the basic flip-flop substantially increases its driving capability and provides isolation from noise in the external load. When inverters are used as the amplifying element, the asserted output cannot be taken from the collector of the cutoff transistor. Instead the buffer inverter driven by the opposite collector provides the output (figure 3-4).

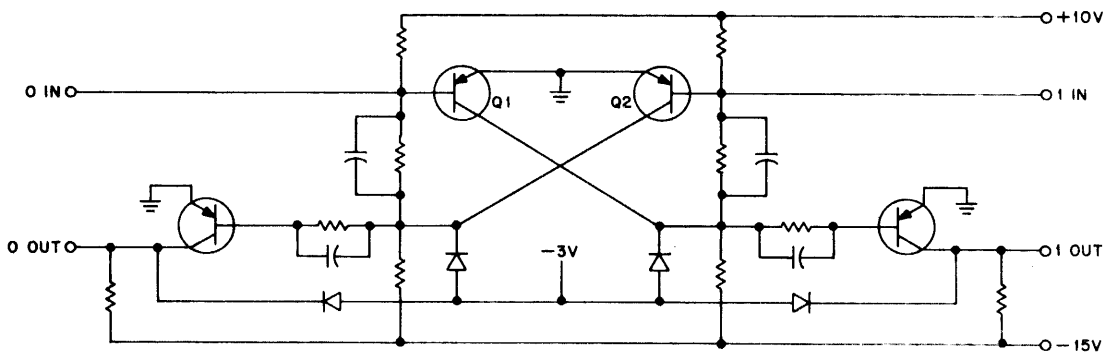


Figure 3-4 Flip-Flop with Output Buffer Inverters

The pnp output buffer transistor is saturated when turned on and therefore has considerable drive capability at ground assertion. At negative assertion, however, the drive capability is limited by the conductance of the clamped load resistor acting as a current sink. When increased drive capability is required at negative assertion, a push-pull output buffer is used. Figure 3-5 shows a basic flip-flop, Q1-Q2, which drives push-pull output buffer Q3-Q4 to develop the negatively asserted 1 output. When the flip-flop is set, Q2 conducts and Q3 is cut off, allowing Q4 to behave as an emitter follower driven by the -3 vdc level from the cutoff Q1 collector. When the flip-flop is cleared, Q1 conducts and Q4 is cut off, allowing Q3 to behave as an emitter follower driven by the -15 vdc level from the cutoff Q2 collector.

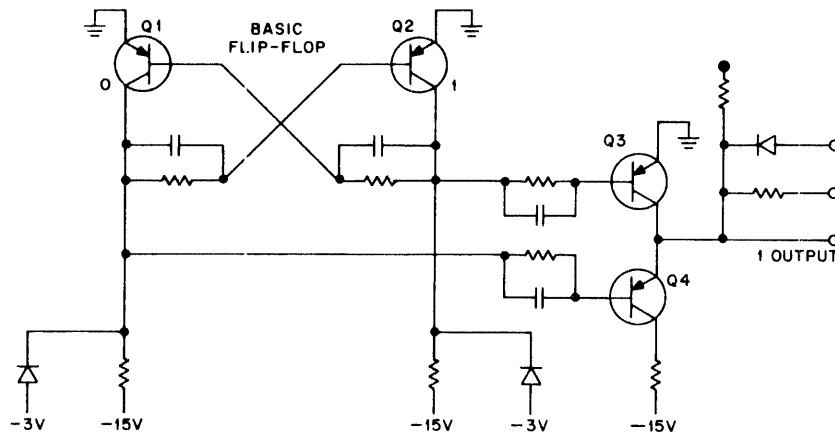


Figure 3-5 Push-Pull PNP Output Buffer

The current drive capability at the negative 1 output to the right of the figure is limited only by the Q4 collector resistance. Since Q4 never saturates, it can release the output for transition to ground level without requiring elimination of minority carrier storage caused by collector saturation. When the flip-flop is cleared, Q1 conducts and Q4 is therefore cut off; the Q2 collector load draws current through the Q3 base resistance to saturate Q3 and negate the 1 output at ground.

Push-pull complementary emitter followers (figure 3-6) are also used when the flip-flop is required to supply large amounts of current to the load at both logic levels. For ground level inputs, Q1 supplies current to the load through R3. The output point is then more negative than the Q1-Q2 base connection because of the forward drop of the Q1 emitter-base diode, and Q2 is therefore biased to cutoff. When the input is held at -3.75 vdc by D1-R2, Q2 conducts current from the load to -15 vdc through R4, and Q1 is cut off. R3 and R4 limit the load currents: this circuit can maintain a ground level up to 80 ma drain and a -3 vdc level up to 120 ma.

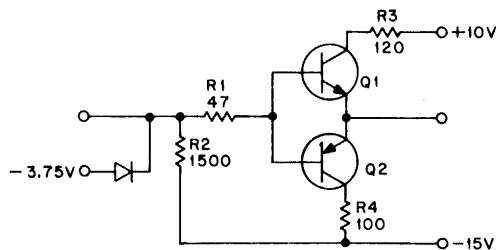


Figure 3-6 Push-Pull Emitter Follower

3.1.4 Pulse Amplifier

Pulse amplifiers (figure 3-7) standardize amplitude and width of carry pulses from one flip-flop in a register to the next. In the pulse transformer-inverter combination shown in figure 3-7, the pulse input point when quiescent is held to -8 vdc by the R1-D1 clamped load, through the low resistance primary of the transformer. The output terminal is at ground. The leading edge of a positive-going input pulse is coupled to the output as a sharp negative step (dots indicate relative winding polarities). A negative step of smaller amplitude is applied to the base of feedback transistor Q1 from the secondary center tap. The transistor amplifies and inverts this portion of the output pulse and returns it to the input, where it maintains ground potential even if the input pulse should prematurely disappear.

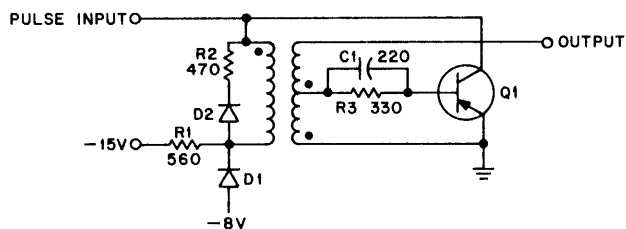


Figure 3-7 Pulse Amplifier

Output pulse width is therefore determined primarily by the pulse transformer and R1. The pulse ends when the transformer primary current reaches the value of current through R1. Current through clamp diode D1 is then reduced to zero, additional primary current increases the voltage drop across R1, and primary voltage begins to fall. The induced base drive to Q1 falls, reducing feedback, and the transformer voltages rapidly collapse. D2 and R2 prevent ringing by dissipating all stored energy in the first back swing after pulse completion.

3.2 1250 FAST MEMORY FLIP-FLOP

The Type 1250 is a quadruple module containing 24 flip-flops, interconnected to form three contiguous bits of eight flip-flop registers. In PDP-6, two groups of twelve Type 1250 modules make up a bank of sixteen 36-bit fast memory registers. Additional circuits include three diode readout gates and three noninverting digit amplifiers. A readout gate comprises eight 2-input negative AND gates with outputs ORed together, amplified and inverted. A digit amplifier is made up of two standard inverter amplifiers which supply incoming data to the register selected by the active write line.

Clear inputs are DEC standard 70-nsec positive-going pulses, applied separately to each register. Write signals are standard negative pulses which trigger the flip-flop collector through input buffer inverters. Buffer inverter emitters in each vertical column are gated by a single digit amplifier with output assertion at ground. Flip-flop registers can be sampled nondestructively and must be cleared before reading. The clear must precede the write by at least 100 nsec. Read signals are standard negative pulses. To sample one of the eight registers, the appropriate read line, ANDed with the 0 outputs of that register by the three diode networks, is pulsed. Transistors Q79, Q80, and Q81 invert the gate outputs, so the output of the sampled register appears at BZ, BL, and AE with negative assertion for 1s.

The operation of the 1250 Flip-Flop is identical to that of the basic flip-flop with one exception: clamped loads to -3 vdc are not used at the collectors of 1250 Flip-Flops. Instead, all flip-flop collectors are referenced through 1500 ohms to the parallel combination of R55 and R56, shown in the bottom right of the schematic. Since half of the 48 load resistors are at all times tied to grounded flip-flop collectors, load resistors for the off transistors operate into a voltage divider between -15 vdc and ground.

3.3 1260 SUBROUTINE CARD

This module contains three circuits, each comprising a flip-flop, a pulse amplifier, and two diode gates. Each circuit provides reentry to an asynchronous time chain by producing a single output pulse upon receipt of a restart pulse while the flip-flop is set (a logic diagram of this module precedes the schematic). The following describes the circuit including Q1 to Q6 and Q19. Flip-flop Q2-Q3 may be set either by grounding H or by applying a -3 v pulse to K. While the flip-flop is 1 (-3 vdc at L, 0 vdc at H), a negative-going pulse or level change at J appears at E, amplified and standardized to 70 nsec duration. The flip-flop is cleared by grounding L or by applying a -3 v pulse to the D1 or D2 cathode at F or E (a pulse at F clears the entire module). Note that the output pulse at E is applied back to the clear input of the flip-flop via D2 and Q1, so once the restart pulse has been received, no further output pulses can be produced until the flip-flop is again set.

The flip-flop used in the 1260 is the basic one discussed above. It is collector-gated with standard input buffer inverters, Q1 and Q4; the D5-D7-Q5 diode gate is also of standard design. The pulse amplifier (Q6-Q19-T1-T2) is similar to that in the Type 1609 Pulse Amplifier-Standardizer.

3.4 4214 QUADRUPLE FLIP-FLOP

The Type 4214 contains four flip-flops, each with both inputs and both outputs available at the connector. Each pair of flip-flops shares a common direct clear input at P or R. The module operates at any frequency up to 1 mc, using the basic flip-flop discussed above, but without internal capacitor-diode gates.

The common clear inputs require DEC standard 0.4- μ sec positive pulses, which must precede readins by at least 1 μ sec. The set and clear inputs to each flip-flop may be driven by positive capacitor-diode gates or by DEC standard 0.4 μ sec positive pulses. Since all 1 and 0 outputs are available, the flip-flops may also be set or cleared at their collectors. Typical flip-flop output delay is 50 nsec.

3.5 4217 FOUR-BIT COUNTER

The Type 4217 contains four flip-flops, a pulse inverter-amplifier, positive capacitor-diode gates, and a negative dc supply. Depending upon external connections, the module may function as a counter or a buffer register with 1s transfer parallel readin. All input signals are applied to the flip-flops through positive capacitor-diode gates such as the C18-R37-D22 combination. The negative dc supply, consisting of D26 to D29 and R41, has a -0.75v tap at the D26-D27 junction and a -2.25v tap at the D28-D29 junction. Two capacitor-diode gates at each flip-flop have a common pulse input and are conditioned by the flip-flop outputs to form a complementing gate. Complement inputs for flip-flops A, B, C, and D are pins X, T, N, and H. Complement and clear signals are DEC standard 0.4- μ sec positive pulses; the readin at F is a 0.4- μ sec negative pulse.

The module may be connected as a 4-bit counter by tying the complement inputs of flip-flops B, C, and D either to the 1 outputs (up counter) or to the 0 outputs (down counter) of the preceding flip-flops. Count pulses are applied to pin X. For example, if the counter is initially clear and is connected for up counting, a pulse at X complements FFA to 1 because the gate is enabled by ground at the Q9 collector. The arrival of a second count pulse at X returns FFA to 0, causing its 1 output to rise to ground. This positive-going transition is coupled through the complement gate of FFB to the Q7 base, and sets FFB. Counting continues in this manner until the counter recycles to all 0s or is cleared by a pulse at E. The count may begin with any desired number, using the parallel readin gates and pulse input F. When the register functions as a down counter, the carry chain must be inhibited while the initial number is read in. A long time constant in the clear circuit prevents carry propagation when the register is cleared (this is necessary in the up count configuration).

3.6 4218 QUADRUPLE FLIP-FLOP

This module contains four flip-flops, a pulse inverter-amplifier, eight positive capacitor-diode gates, and a negative dc supply. Depending upon external connections, the Type 4218 may be used as a

shift register, or buffer register with jam transfer parallel readin. All input signals arrive at the flip-flops through positive capacitor-diode gates such as the D1-C11-R29 combination. The negative dc supply, consisting of D17 to D20 and R28, has a -0.75v tap at the D17-D18 junction and a -2.25v tap at the D19-D20 junction. The readin at P is a DEC standard $0.4\text{-}\mu\text{sec}$ negative pulse. Levels at E, H, S, and V gate the pulse at the set inputs of the flip-flops; levels at F, K, U, and X gate the pulse at the clear inputs. Gating levels must be present at least $1\ \mu\text{sec}$ before readin for assertion (ground) and $2\ \mu\text{sec}$ for negation. All four flip-flops are cleared simultaneously by a DEC standard $0.4\ \mu\text{sec}$ positive pulse at R. A clear pulse must precede a readin by at least $1\ \mu\text{sec}$. Total flip-flop delay is less than or equal to $50\ \text{nsec}$.

For readin, complementary levels are connected to the two input gates of each flip-flop. The readin pulse thus loads (or shifts) 0s and 1s simultaneously, regardless of the prior states of the flip-flops.

3.7 4220 EIGHT-BIT BUFFER

This module contains eight flip-flops, each with positive capacitor-diode readin gates, a negative dc supply, and two pulse inverters, one to clear the flip-flops, the other to drive the gates. The gate driver inverter output is applied to an emitter follower whose low impedance output prevents cross coupling between capacitor-diode gates. For each flip-flop, the 1 input and a single output are available at the module connector. An output pin may, however, be connected either to the 1 or to the 0 output eyelet of its associated flip-flop with an internal jumper. The jumper code is an octal number representing an 8-bit binary number that identifies the output used for each flip-flop.

The clear and readin inputs require DEC standard $0.4\text{-}\mu\text{sec}$ negative pulses. A clear pulse must precede readin by at least $1\ \mu\text{sec}$. Level inputs are DEC standard signals, asserted at ground through positive capacitor-diode gates. Gating levels must be present at least $1\ \mu\text{sec}$ before readin for assertion and $2\ \mu\text{sec}$ for negation. Total flip-flop delay is less than or equal to $50\ \text{nsec}$.

3.8 4221 SIX-BIT SHIFT REGISTER

This module comprises six flip-flops, positive capacitor-diode gates, three pulse-inverter amplifiers, and a negative dc supply. The flip-flops are internally connected as a shift register and may be preset with a 1s transfer parallel readin. All signals are applied to the flip-flops through positive capacitor-diode gates such as the C1-R2-D42 combination. The negative dc supply, consisting of D34 to D37 and R5, has a -0.75v tap at the D36-D37 junction.

Clear, shift, and readin pulses at Z, X, and Y respectively are DEC standard $0.4\text{-}\mu\text{sec}$ negative pulses. The output of readin inverter Q15 drives npn emitter follower Q16, which provides a low impedance signal to prevent cross coupling between capacitor-diode gates. Pins R, S, T, U, V, and W are the

parallel inputs and are asserted at ground. Gating levels must be present at least 1 μ sec before readin for assertion and 2 μ sec for negation. A clear pulse must precede readin by at least 1 μ sec. Total flip-flop delay is less than or equal to 50 nsec.

Flip-flops 1 to 5 have single output terminals (H, J, K, L, and M); each may be jumpered internally to either the 1 or the 0 output of the associated flip-flop. Both outputs of flip-flop 6 are available at the connector. An additional jumper provision allows the clear line to be connected either to the set or clear input of flip-flop 1. The octal number in the jumper code therefore represents a 5-bit binary number that indicates which flip-flop outputs appear at the connector. The number is followed by S or C to denote the connection of the clear line to flip-flop 1.

3.9 4225 EIGHT-BIT COUNTER

The Type 4225 contains eight flip-flops with complement inputs internally connected in a counter configuration, a single inverter used for presetting, and a negative dc supply. Both collectors of each flip-flop are available at the module connector and serve both as inputs and outputs. A series of jumper connections in the complement circuits of the register allows a choice of either binary or BCD counting (appropriate connections are indicated by B and D at the jumper eyelets). Flip-flops 4 and 8 have separate set and clear gates, rather than single complement gates, to facilitate alternate counter connections. For either mode, pin Y is the LSB count input and accepts a standard 0.4- μ sec positive pulse or positive-going level change. The complement network for each flip-flop comprises two capacitor-diode gates with a common pulse input. The gates are conditioned by the flip-flop outputs. The preset inverter, Q17, accepts a negative pulse of 1 μ sec minimum duration at Z. The pulse is inverted and applied through a capacitor-diode network to eight jumper eyelets. The register may be preset in any desired way by jumpering these eyelets to the appropriate flip-flop bases. The octal number in the jumper code represents the 8-bit number to which the module is preset. The number is followed by B or D to indicate binary or decimal operating mode.

3.10 4706 EIGHT-BIT TELETYPE RECEIVER

This module contains 14 flip-flops and a one-shot multivibrator (pulse shaper), with all gating implemented by positive capacitor-diode networks. Eight of the flip-flops make up a shift register; the remainder perform various control functions associated with the transfer of 8-bit Teletype characters from a unipolar line into the shift register. An 880-cps clock provides all timing at S. Usually the maximum transfer rate is 10 characters per second. The 100-msec period required for a single character transfer is divided into eleven equal unit intervals as follows:

START--one unit

8-bit character--eight units

STOP--two units (or more; prolonged STOP indicates idle line)

A timing diagram and a modified logic diagram accompany the schematic.

Between transfers, the Teletype receiver is inhibited by the STOP signal (ground) at T, holding the D26 cathode negative and inhibiting the ACTIVE set gate. Pin U must be at ground to enable the module. When START (-3v) arrives at T, the D26 cathode is grounded through inverter Q33, allowing R65 to enable the ACTIVE set gate. The following clock pulse at S sets ACTIVE, inhibiting the diode gate at the D24 cathode and generating a preset pulse through Q35 and its associated capacitor-diode gate. The preset pulse sets all shift register bits; it clears IN LAST UNIT and the MSB of the 3-bit counter (the other two are both 0 at this time). Since the counter is enabled when ACTIVE is 1, the next clock begins the first 8-count cycle. Every 4-count triggers the shift one-shot input gate, which is conditioned by the 0 state of IN LAST UNIT. The single pulse resulting at the Q24 collector is inverted by Q22, amplified by npn emitter follower Q21, and applied to the shift register input gates. Since 1 inputs at T are asserted at ground, the first shift transfers START into the register as a 0; the next eight pulses shift in the character. After seven bits have been read, the 0 in IN1 enables the set gates to IN LAST UNIT and FLAG: the eighth shift thus sets both flip-flops (FLAG lights an indicator mounted on the module). The 1 state of IN LAST UNIT inhibits the shift one-shot and enables the ACTIVE clear gate, C2-D31-R76, so the next 4-count clears ACTIVE. Since the STOP level (ground) is now present at T, the receiver is disabled until the arrival of the next START. For a standard 2-unit STOP code, jumpers C and D are present. IN LAST UNIT then enables the counter for one more cycle until the next 4-count clears it (this is the case shown in the timing diagram). For 1-1/2 units, B and D allow the next 0-count to clear IN LAST UNIT. For a 1-unit code the same 4-count that clears ACTIVE also clears IN LAST UNIT because of jumpers C and E. In any case the counter is inhibited when IN LAST UNIT clears, so it stops with the two less significant bits clear.

Transient inputs at T are prevented from activating the receiver by a diode gate which samples the outputs of all shift register bits and the pin T input. If the START level does not persist for at least five clock pulses, R64 enables an auxiliary ACTIVE clear gate, C23-R80-D32, which is pulsed by the first SHIFT, deactivating the receiver.

The flip-flops and positive capacitor-diode gates used in the 4706 module, as well as the npn emitter follower (Q21), are discussed at the beginning of this chapter. The one-shot multivibrator, comprising Q23 and Q24, is similar to the standard bistable multivibrator, or flip-flop, with the exception that no dc path exists from the Q23 collector back to the Q24 base. The device is therefore capable of only one stable state, in which Q24 conducts and Q23 is cut off. A positive pulse applied to the Q24 base momentarily cuts off Q24, driving Q23 into conduction. The positive transition at the Q23 collector is

coupled through C2 back to the Q24 base. The C2-R6 time constant primarily determines the duration of the negative level at the Q24 collector. As C2 discharges through R6, Q24 is eventually biased back into conduction and reverts to its quiescent state.

There is only one output terminal for each character flip-flop, and it can be connected to either the 1 or 0 side with an internal jumper. The jumper code thus includes an octal number equivalent to eight bits which indicate the outputs used. Following the number an F indicates a jumper that causes FLAG to be cleared when reception of a new character begins; an A indicates a jumper that allows ACTIVE to be sampled at pin M; and the letters associated with the STOP code jumpers indicate which of those are present.

3.11 4707 EIGHT-BIT TELETYPE TRANSMITTER

The Type 4707 Transmitter receives 8-bit characters from the PDP-6 I/O bus and sends out each character serially as a Teletype signal on a unipolar line. The module comprises 15 flip-flops and associated inverter and positive capacitor-diode logic. Ten flip-flops are connected as a shift register; the remainder perform various control functions associated with the character transfer. Timing is governed by a 220-cps clock input at T. Usually the maximum operating speed is 10 characters per second. The 100-msec cycle is divided into eleven equal units as follows:

START: one unit

8-bit character: eight units

STOP: two units (completing the cycle; longer indicates idle line)

A modified logic diagram and a timing diagram are included with the schematic. The module uses the basic flip-flop, capacitor-diode gate, and npn emitter follower discussed at the beginning of the chapter.

The transmitter is inactive until readin occurs at N, loading a character into the 8-bit OUT register and setting ENABLE, which in turn conditions the ACTIVE set gate through the D59-D61-D62 gate. The next clock sets ACTIVE, enabling the set input gate of a complementing flip-flop (FREQ DIV) and clearing OUT LINE to generate the START level at V. Subsequent clocks trigger the frequency divider, which generates a shift pulse through inverters Q23, Q22, and emitter follower Q21 on every transition to 0. The first shift moves the initial 1 from ENABLE into OUT8, shifts the character one place to the left, and sends out the first character bit by shifting OUT1 into OUT LINE. Each shift sends out a bit and clears ENABLE, so 0s follow the initial 1 through the register. The eighth shift places 1 in OUT1, followed by 0s in the remainder of the register and in ENABLE. This condition enables the ACTIVE 0 input through the large diode gate; thus the next and last shift clears ACTIVE while shifting 1 into OUT LINE.

The signal now at pin V is the STOP level, which usually must persist for at least four clock pulses. This time interval is supplied by a pair of STOP flip-flops that furnish a 4-count in the sequence 01, 11, 10, 00, provided jumpers A and B are present (this is the case shown in the timing diagram). The

0 transition in ACTIVE, besides setting FLAG (which lights an indicator mounted on the module), also sets OUT S1. The next three clocks continue the count, of which all steps except 00 inhibit the ACTIVE set gate in case a new readin has already occurred. The transmitter is reactivated by the first clock following the 00 count or a readin, whichever happens later. However, a negative level at R extends the inhibit indefinitely by holding OUT S1 on.

For a STOP code of 1-1/2 units, jumpers A and C enable the ACTIVE set gate at the same configuration, but the STOP flip-flops cycle through a 3-count: 01, 10, 00. For a 1-unit code, the absence of A enables the set gate on OUT S1(0), and C causes OUT S1 to set and clear on two clocks.

Either polarity may be selected at output V (and its opposite at W) by jumpering the desired OUT LINE output to the Q41 base. The jumper code thus includes a 0 or 1 to indicate the output used. An F indicates a jumper that allows FLAG to be cleared when a new character is received; the letters associated with the STOP code jumpers indicate which of those are present.

3.12 6203 SC AND FE FLIP-FLOPS

This module contains two 10-mc flip-flops, the 1th bits of the 9-bit shift counter and floating exponent register. It is double size and is serviced by two standard 22-pin connectors (rear connector pin designations have the prefix R). A tap on the load resistance for the internal -3 vdc supply provides -8v for the pulse transformer primary clamp.

A logic diagram for the 6203 module, showing transistor numbers, is included with the schematic. In addition to standard inverter and diode gates, three special circuits are associated with the basic flip-flops and output buffers (all are discussed at the beginning of the chapter). Npn emitter followers Q11 and Q19 change SC state directly by grounding the appropriate flip-flop collector. The LC networks at the Q11 and Q19 bases delay the state change about 50 nsec from the leading edge of an incoming trigger pulse. The SC complement network, shown in the lower half of the logic diagram, operates entirely through this pulse delay to prevent race conditions. A pulse amplifier (upper left) is used for SC carry propagation.

Transistors Q12 and Q20 make up the basic SC flip-flop; Q8 and Q22 are its output buffers. A direct set input is provided at T, which triggers the flip-flop through npn emitter follower Q24; this input requires positive-going pulses from a pulse inverter, and includes the clamped load. SC may be cleared at RL through the pulse delay by a DEC standard 40-nsec negative pulse. The 1 and 0 outputs are at M and L; the resistor-coupled output at R may drive an indicator amplifier.

The FE flip-flop is unbuffered and may clear directly at the Q34 base by applying a 40-nsec positive pulse to RE. It may be set at < by a level or positive-going pulse to ground. The J output is resistor-coupled for connection to an indicator driver.

3.13 6205 ARITHMETIC REGISTER FLIP-FLOPS

This module contains four flip-flops, each the *i*th bit of one of the 36-bit processor registers, AR, MQ, MB, and MI. It also includes AR carry circuits. The module is triple size (in area) and is serviced by four standard 22-pin connectors. Pin designations are two letters, the first naming the connector (A, upper front; B, lower front; R, upper rear; S, lower rear), the second naming the pin. On the processor logic diagrams the front connectors are labeled by mounting panel. The internal -3 vdc supply for this module is derived from four series-connected silicon diodes, loaded to -15 vdc. A tap on the supply load provides -8v for the pulse transformer primary clamp. Three logic diagrams with transistor numbers for all flip-flops in the 6205 module accompany the schematic.

MI flip-flop logic, shown with MB, is considerably simpler than that of the other three, since MI is required only to store a memory bit and drive an indicator circuit. It is set by the 1 state of MB and a negative pulse at SN, through an input pulse inverter Q30. A negative pulse at SR clears the flip-flop through Q1; output point BS includes a series 3K resistor to drive the indicator.

Most of the input circuitry on AR, MB, and MQ consists of inverter networks that implement the many set and clear conditions required by logical, arithmetic, and transfer operations. All pulse inputs to the three flip-flops are bused to the rear connectors (R and S) from the arithmetic Bus Driver 6615, which produces 25-nsec pulses instead of the usual 6000-series 40-nsec pulses. To prevent race problems, flip-flop response time is carefully standardized at manufacture to ensure approximately 50-nsec delay between the input pulse leading edge and the signal response at the flip-flop output buffers. All input level conditioning is performed by the buffers (the basic flip-flop drives only the buffer), consequently input gating conditions cannot change until somewhat after the trailing edge of a pulse that changes the flip-flop state.

Trigger circuits on the 6205 differ from those on other modules: an emitter-driven pnp stage drives both basic flip-flop transistor bases through a pulse transformer. The clear and set triggers for all three flip-flops are identical; e.g., the clear trigger for AR (at the right in the schematic) consists of Q58 with pulse transformer T5. The Q58 base is clamped to -3.7v while its collector is loaded to -15v through the T5 primary. When one of the clear gates (at the top) is pulsed, it pulls the Q58 emitter toward ground so that Q58 saturates, placing approximately 13v across the T5 primary. The LC network at the Q58 collector introduces a short delay which adds to the transition time of input inverters, flip-flop, and output buffers to give the total flip-flop transition time. The T5 secondary simultaneously turns on Q74 through D29 and turns off Q75 through D31. Since both flip-flop transistors are pulsed, the output buffers provide simultaneously changing signals when the flip-flop is triggered.

The basic flip-flops, output buffers, and register clear inputs for AR, MB, and MQ are identical; all are 10-mc types using the push-pull pnp output buffer, and each has additional npn emitter-follower

input triggers that change flip-flop state by shorting the appropriate collector to ground. The emitter-follower pulse inputs at the front connectors are the only inputs that do not use the pulse amplifier trigger circuit described above. Clamped loads are included at the emitter-follower bases for the required external pulse inverters.

The AR circuits include an output pulse amplifier with additional networks for carry output gating and carry completion detection. The pulse amplifier consists of Q64 and pulse transformer T7 in the configuration described at the beginning of this chapter. If AR is 1, it delivers a 25-nsec negative pulse at AF when an input pulse appears at AH. The output is also triggered by a negative pulse at RH, if AR is 0 and MB is 1. These conditions are set up at two transistor AND gates, Q60-Q62, and Q61-Q63. A parallel output at AE is ORed with its counterparts on all other 6205 modules through D59 to detect the carry output; AE is therefore at ground potential only when carry propagation has terminated.

3.14 6206 MA, PC, AND IR FLIP-FLOPS

This module contains three flip-flops, the *i*th bits of the 18-bit processor registers, PC, MA, and IR. The module is double size and is serviced by a standard 22-pin connector at each end (rear connector pin designations have the prefix R). A tap on the load resistance for the -3 vdc internal supply provides -8v for the primary clamps of two pulse transformers. A logic diagram with transistor numbers is included with the schematic.

The MA flip-flop input circuits consist primarily of inverter networks that implement the memory address transfer logic. The diode comparison gate shown at the bottom of the logic diagram generates an output at K if the state of MA is the same as that of the corresponding memory address switch. Other MA circuits include a count net which complements the flip-flop through a delayed trigger circuit (Q15-Q23) when pulsed at P, and also generates a carry at N if MA contains 1.

The PC flip-flop circuits consist simply of a complement-carry network driving a pulse amplifier similar to that of MA, and a PC set gate. E is the count input for this flip-flop, and F is the carry output.

IR flip-flop circuits consist of a simple direct set network and two pnp-npn push-pull emitter-follower amplifiers (Q1-Q2 and Q10-Q11), one at each flip-flop output.

All 6206 circuits, including buffered and unbuffered flip-flops, npn emitter followers, push-pull emitter-follower amplifier, and pulse amplifier-standardizer, are discussed at the beginning of the chapter.

3.15 6227 EIGHT-BIT BUFFER

This module contains eight 10-mc flip-flops with no interconnections other than a clear line. Two inverters are provided for clearing: one, with input connection at P, clears a minimum of four and

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a maximum of seven flip-flops; the inverter driven at R clears a minimum of one and a maximum of four. Clear signals at P and R are negative-going transitions resulting from level changes or DEC standard 40-nsec negative pulses; they are applied through Q17 and Q18 to the bases of the appropriate transistors. Positive-going levels or pulses applied directly to the flip-flop collectors can be used for individual setting and clearing.

Flip-flops with outputs T-S, V-U, and W-X may be cleared through either Q17 or Q18, depending upon internal jumper connections. Jumper identification for this module is therefore a 3-symbol code, one for each ambivalent flip-flop. P or R indicates the input connection; 0 indicates no connection.

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CHAPTER 4 AMPLIFIERS

Amplifier types in the PDP-6 fall into two categories, pulse amplifiers and level amplifiers. The former are used not only to amplify short duration signals but also to shape and standardize them in amplitude and width; circuits for these modules are characterized by toroidal-core transformers, which generate pulses at relatively high currents with very short rise times. The level amplifiers are special-purpose modules usually associated with the in/out system and the memory bus; they function as solenoid, bus, and indicator drivers.

All PDP-6 pulse amplifiers except the Type 4606 operate in either the 5- or 10-mc speed range and must be driven by the collector of an inverter, which may be included on the module. The input to the base of this inverter must be a negative-going signal with an amplitude between 2 and 5v. For all 6000 series modules and for the Type 1609, the fall time of the negative pulse or level change must be less than 25 nsec; duration at 2v must be greater than 25 nsec. The remaining 1000 series modules require a fall time less than 50 nsec and a width greater than 50 nsec at 2v. Delay through a 5- or 10-mc pulse amplifier is approximately 25 nsec. The Type 4606 can be triggered by 2.5-4v level changes or pulses, of either polarity, having a rise (or fall) time less than 0.4 μ sec and a duration at 2v greater than 70 nsec. For any PA, pulse amplitudes less than 0.5v cannot result in an output pulse. In general, a pulse amplifier produces output pulses characteristic of its speed line: 0.4 μ sec, 70 nsec, and 40 nsec for the 4000, 1000, and 6000 series, respectively.

4.1 BASIC PULSE AMPLIFIER

To avoid repetition, this section describes a basic pulse amplifier that with minor variations forms a part of five modules. The schematic of figure 4-1 shows two input inverter configurations. Normally Q1 drives T1 directly. When Q1 is a high speed transistor (such as the MD94) with a breakdown rating below 8v, but the needed drive power to Q3 requires a -8v clamp at the T1 primary, common base stage Q2 is added to provide voltage standoff to Q1. The Q2 emitter (and Q1 collector) can go no more negative than -4.5v.

Under quiescent conditions, the transistor driving T1 terminal A is cut off so the T1 primary is held to -8 vdc by the D4-R4 clamp. Since no current flows in the T1 secondary at this time, Q3 is open circuited with its base and emitter at ground, and no current flows in the T2 primary. When A is pulled up to ground from its previous -8v level, the T1 primary inductance initially impedes current flow through it and R4 to the -15v supply, while the increasing magnetic field develops a sharp current pulse in the secondary (dots indicate the more positive winding polarities during the pulse). Q3 is immediately saturated

by this pulse, whose current amplitude is approximately proportional to the rate of change of the T1 primary current. As the R3-R4 junction rises toward ground potential, the primary current building toward the steady state maximum (10 ma in this case) proceeds more slowly, with a corresponding decrease in the T1 secondary current and voltage, until conduction through the Q3 base-emitter junction can no longer be maintained and Q3 cuts off. When the ground at A is removed, the reverse current spike generated by the T1 primary is damped out through R3 and D3. In addition to the inductance of the T1 primary and secondary, two other factors are primarily responsible for determining pulse width at the Q3 collector: the silicon V_{be} of Q3, and the emitter to ground potential established by R6. Increasing R6 decreases the pulse width and reduces T1 secondary current. Transformer T2 provides current amplification of the pulse generated at the Q3 collector. Positive output pulses are available at the T2 secondary when the negative terminal is grounded and vice versa. R5 and D5 damp the T2 primary backswing in the same manner as D3-R3.

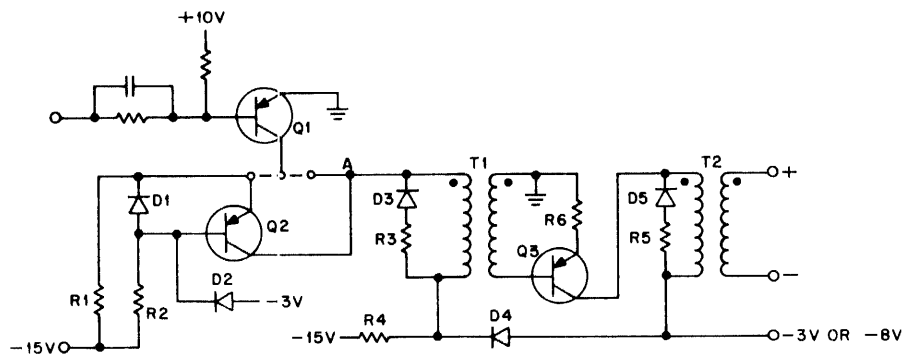


Figure 4-1 Basic Pulse Amplifier with Two Typical Driving Circuits

4.2 1607 PULSE AMPLIFIER

This module contains three of the basic pulse amplifiers (common-base input circuit) and three input inverters. The amplifiers, Q2-Q3, Q5-Q6, and Q8-Q9, are driven at H, L, and P. Their outputs are available at E-F, J-K, and M-N. Inverters Q1, Q4, and Q7 can be used in series for logic gating or with grounded emitters as individual triggering inputs. The triggering input to an inverter base is usually a DEC 70-nsec negative pulse, but the input requirement is satisfied by any negative transition meeting the specifications cited in the introduction to this chapter. The output generated by this signal is a DEC standard 70-nsec pulse, delayed by 25 nsec and capable of driving 16 units of pulse load.

Each amplifier has a separate 8v supply provided by a low-resistance voltage divider between -3 and -15 vdc (example: R11-R16). Capacitors such as C2 and C4 flatten the pulse top by maintaining a high rate of change of primary current for a longer time.

4.3 1608 PULSE AMPLIFIER

The Type 1608 contains two dual-output pulse amplifiers and two input inverters. The amplifiers are the basic type (common-base input circuit) with a duplicated second state. They are Q2-Q3-Q4 and Q6-Q7-Q8, and are driven at K and R. Outputs of the first are available at H-J and E-F; those of the second at N-P and L-M. Inverters Q1 and Q5 can be used in series for logic gating or with grounded emitters as individual triggering inputs. Input and output characteristics and all circuit parameters are identical to those of the Type 1607, except for the dual output stage that allows a single input pulse to produce a pair of output pulses of the same or opposite polarities. Since each pulse amplifier output is an independent transformer winding, transformers may be connected in parallel to increase the driving current, or in series to increase the pulse voltage amplitude for special purposes. Each output can drive 16 units of pulse load.

4.4 1609 PULSE AMPLIFIER

The six pulse amplifiers contained in this module differ from other PDP-6 pulse amplifiers by using feedback networks to transform very short-duration pulses into standard DEC 70-nsec signals. The Type 1609 is therefore useful as an interface between the 1000 and 6000 series. The amplifiers, Q1-Q2, Q3-Q4, Q5-Q6, Q7-Q8, Q9-Q10, and Q11-Q12, are driven at E, J, M, R, U, and X. Their outputs are available at H-F, L-K, P-N, T-S, W-V, and Z-Y. Pulse transformers in this module are referenced through suitable resistors directly to -15 vdc rather than to an intermediate negative supply. The internal -3 vdc source is loaded through 195 ohms to the -15 vdc supply, maintaining approximately 60-ma no-load current through the four series diodes. This relatively high current level reduces transients that occur on the -3v line when inputs are pulsed.

Pulse amplifier inputs must be driven from the collectors of one or more pulse inverters. The signal at the pulse inverter base must have a rise time less than 25 nsec; pulse width (at 2v) may run from 25 nsec up. When these input conditions are met, the output is a DEC standard 2.5v 70-nsec pulse that is negative if the positive terminal is grounded and vice versa. Outputs can drive 10 units of pulse load each and should not be used without terminating resistors. Although resistor values are ultimately dependent upon line length, 47 ohms is approximately correct when driving 1-5 units; 82 ohms is generally used to drive 6-10 units.

Consider the Q1-Q2 circuit as typical. It differs from the basic pulse amplifier in two respects: the T1 and T2 primaries are not clamped to -8 vdc, and the feedback circuit of Q1 has been added. To ensure a 70-nsec output from a pulse source as short as 25 nsec, Q1 is effectively placed in parallel with the driving source. A portion of the pulse amplifier output is fed back to the Q1 base by a separate T2 secondary winding. This signal saturates the transistor, maintaining the ground level at E for 70 nsec, when the circuit constants end the pulse. Capacitors C1 and C2 aid in flattening the output pulse top.

4.5 1664 MEMORY BUS CONTROL

This module contains four gated pulse amplifiers and a 7-input AND gate for positive signals (expandable to 9). It is quadruple size, with four 22-pin connectors, and has been designed specifically for use in the PDP-6 two-way memory bus system. The Type 1664 accepts a DEC standard 70 nsec negative pulse or a level change meeting the requirements for the 1000 series set forth in the beginning of this chapter. Each pulse amplifier output drives the center of a 93-ohm coaxial cable (50 ohms dc to ground) with a 100-nsec negative pulse.

Type 1664 modules are used in PDP-6 memory to decode the most significant bits of a processor memory address and, after priority system recognition, to implement various control and timing functions between the addressed memory and the processor having current access. PDP-6 can include a maximum of four processors and every memory must contain one 1664 for every processor. The address of a given memory is wired into its 1664s by jumpering the appropriate memory address lines (asserted at ground) at K or L, M or N, P or R, and T or U to four of the decoder gate inputs.

When 8K rather than 16K banks are used, an additional address line may be selected at V or W to accommodate a larger number of memories. Replacing 16 locations in core with a fast memory requires further access to the decoder at X or Y. The 8K and fast memory inputs may be gated separately and brought out to BC, or may be joined with the remaining decoder inverters, with output at BT. Two remaining inputs to the decoder indicate memory ready (BR) and a processor request for memory (RF). Since the latter is asserted negative, it is inverted before being applied to the decoder.

A negative output at BP therefore indicates a processor request for the memory to which the module is assigned; this signal is routed to the priority system, which grants access to the processor by enabling the level input to the four pulse amplifiers on the module--BW, AH, BU, and AM. Subsequent negative memory timing pulses at BY, AE, BS, or AK are placed on the memory bus at B, C, D, or E of either connector and may be gated with negative levels at BZ, AJ, BV, or AN to produce pulse outputs at BX, AF, BT, or AL; the negative level inputs may also gate information from the bus to the pulse output terminals.

The four pulse amplifiers on the 1664 module, of which the Q1-Q2-Q3 circuit is typical, differ considerably from other PDP-6 pulse amplifiers in that a blocking oscillator technique is used to provide the high energy pulses and virtually zero quiescent load required by the memory bus--a feature impossible to duplicate with conventional pulse transformer outputs. The blocking oscillator proper consists simply of T1, Q3, R4, R5, R7, and R8. The Q1 collector is the oscillator input; D1-D4 form a standard negative diode gate which drives the Q1 base through inputs BY and BW. The oscillator output at the Q3 collector is gated with BZ by a similar diode-transistor network to produce ground assertion at the Q2 collector, pin BX.

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The 100-nsec negative pulse is produced by T1 and Q3 as follows: under quiescent conditions (Q1 cut off), approximately 3.6 ma flows from ground through R5, R4, T1, and the parallel combination R7-R8 to the 15 vdc supply. The transformer primary is the winding in series with 750 ohms; the secondary is placed directly across the Q3 base-emitter junction. Since the dc resistance of the T1 windings is low, both base and emitter of Q3 are at nearly the same potential (approximately -14.5 vdc), so that Q3 is cut off. When Q1 is gated on, its collector rises to ground, effectively shorting R5. The Q3 base voltage therefore becomes positive, saturating Q3. The Q3 collector is pulled up to approximately -2.8v if load impedance is 50 ohms. At this time there is approximately 12v across R8 and across the series combination of R7 and the T1 primary. Current in the primary sets up an increasing magnetic field, which is coupled to the T1 secondary to maintain the voltage at the Q3 base. A large amount of positive feedback is coupled across T1 in this manner, keeping Q3 in saturation while current flow increases through the T1 primary. As the rate of current increase lessens, being limited by R7, induced current in the T1 secondary starts to drop until Q3 goes out of saturation, whereupon the rapidly collapsing primary field accelerates Q3 cut-off and the pulse ends. Although a degree of interaction exists between R7 and R8, R7 functions primarily to determine output pulse width by limiting current through the T1 primary, whereas R8 limits output pulse amplitude. Pulse overshoot is damped in the conventional manner by D5 and R3.

4.6 1665 PULSED BUS TRANSCEIVER

This module is quadruple size and, like the Type 1664, is designed specifically for use in the PDP-6 two-way memory bus system. It comprises 18 blocking-oscillator pulse amplifiers, each with two-input negative AND gates at both input and output. The circuits of the Type 1665 Pulse Amplifier are identical with that of the 1664, although the two modules function differently in the system. Type 1665 modules control and amplify the two-way flow of data at either end of the memory bus: between the bus and a processor and between the bus and a memory. Since each module handles 18 bits, two 1665s are required for data at each processor, and two per processor at each memory. Furthermore, each memory requires an additional 1665 per processor to handle the receipt of addresses, but for this application only the output AND gates are used.

The Q1-Q2-Q3 network is a typical one. Q3 and D6 to D9 form a standard NAND configuration for negative inputs; this gate is driven at BV and BX (the latter is common to all input gates on the module). The pulse amplifier output connects directly to the bus and to one input of a similar NAND with output at BW (the second input to this gate, BY, is common with corresponding inputs on all other pulse amplifier output gates). In a processor or fast memory, data is made available to the bus from a flip-flop register. Therefore a level at BV represents a bit to be transferred, and the transfer occurs when BX is pulsed. A data pulse on the bus at RB is brought in through the output gate at BW when a negative level

is present at BY. In a core memory, single data bits are represented by pulses from the sense amplifiers and the read is destructive, so information sent out must usually also be routed to interim flip-flop storage for later rewriting. Thus a pulse at BV is gated onto the bus by a level at BX, and a pulse going in either direction on the bus--that is, a pulse produced by the pulse amplifier or one coming in on RB--can be brought in to BW by a gating level at BY.

Both core and fast memories receive addresses through 1665s using only the output gates. A processor applies the address register levels to the bus, and these incoming levels are pulsed through the output gates at CY.

4.7 4606 PULSE AMPLIFIER

This module contains three pulse amplifiers which produce DEC standard 0.4- μ sec, 2.5v pulses. Each circuit comprises a monostable multivibrator and an output pulse amplifier. It may be triggered at the appropriate input by 2.5-4v level changes or pulses of either polarity, having a rise time less than 0.4 μ sec and a duration at 2v greater than 70 nsec. Maximum operating frequency is 1 mc.

Each pulse amplifier accepts three inputs: a positive pulse, a negative pulse, or a gated negative pulse; each input is one unit of pulse load. A level change of the same polarity can replace the pulse at any input. The gated pulse input is enabled by applying a DEC standard -3 vdc level to the gate level input; this level must be present for at least 1 μ sec before the pulse arrives. When a signal meets the input requirements, the pulse amplifier delivers a positive-going output pulse if the negative terminal is grounded and vice versa.

Each amplifier, e.g., Q1-Q4, comprises a monostable multivibrator (Q1 and Q2), an input pulse inverter (Q3), and an output pulse amplifier (Q4). Capacitor-diode C1-D1 couples a negative input at E to the Q2 base; C7 couples a positive input to the Q3 base, and the resulting negative pulse at the Q3 collector is applied directly to the Q2 base. Thus an appropriate pulse at either input triggers the multivibrator with a negative pulse. The negative output pulse from the multivibrator is amplified by the Q4 circuit; the amplifier output is negative at H if J is grounded, positive at J if H is grounded.

L and K provide an additional, capacitor-diode input to the amplifier. A capacitor-diode gate couples an input pulse to its output when (and only when) an input gating level is asserted. For example, in order to couple a negative pulse at K to the Q2 base, a -3v level must be present at L. When L is at ground, the C5-R13 junction is near zero potential. Since the D6-C6 junction is quiescently at -3 vdc, a negative pulse at K cannot forward-bias D6. A -3v level at L, however, results in 0v across D6, so a negative pulse at K is coupled by D6 and C6 to the Q2 base.

Quiescently, Q1 is on; Q2 and Q4 are off. Base current for Q1 flows through R5 to the -3 vdc supply, holding Q1 in saturation. Voltage divider R2-R6 maintains a small positive voltage at the Q2 base,

keeping Q2 cut off. D2 clamps the Q2 collector to -3 vdc. Voltage divider R3-R4-R7 biases the Q4 base positive, holding it off. The Q4 collector potential is approximately -7 v, as determined by voltage divider R10-R11. No current flows in the T1 primary, and no voltage exists across the secondary.

When a negative pulse appears at input E, C1 and R1 differentiate its leading edge, generating a negative pulse at the D1 cathode. D1 is now forward biased, so the signal appears at the Q2 base. As Q2 turns on, its collector voltage jumps from -3 v to ground. This positive step is coupled by C2 to the Q1 base. Q1 now cuts off and its collector potential drops to -3 v. R6 holds Q2 on, even though the input pulse has ended. The multivibrator remains in this state until the coupling capacitance from the Q2 collector to the Q1 base discharges. Discharge time is proportional to capacitance and is approximately 0.4 μ sec. At the end of this interval, Q1 turns on, cutting Q2 off, and the multivibrator returns to its quiescent state.

The negative pulse generated at the Q1 collector turns on Q4, whose collector rises to ground, placing approximately 7 v across the T1 primary. C4 flattens the pulse top by maintaining a high rate of change of primary current for a longer time (secondary output voltage is proportional to the rate of change of primary current). The pulse terminates when the multivibrator returns to its quiescent state, cutting off Q4. D5 and R18 clamp the T1 primary overshoot.

A positive pulse at F (inverted by Q3) or a gated negative pulse at K triggers the same chain of events to produce an output pulse across J and H. D8 and R15 form a clamped load to -3 vdc which can be connected with an internal jumper to the positive input line. The presence of a jumper is indicated by a 1 in a 3-bit number (written as a single octal digit) in which the bits left to right correspond to inputs F, N, and V.

4.8 6603 PULSE AMPLIFIER

This module contains three 10-mc pulse amplifiers of the basic type (common-base input circuit) and three input inverters. All circuit details and pin connections are identical with those of the Type 1607, the only differences being operating speed and the method of obtaining the -8 vdc source for the pulse amplifier primaries. The Type 6603 produces a DEC standard 40-nsec output pulse, delayed by 25 nsec and capable of driving 12 units of pulse load. Input signals to the base of the driving inverter must conform to the specifications outlines in the beginning of this chapter for 6000 series modules. A 4.7v zener diode, D24, is placed in series with the standard -3 vdc internal supply, resulting in a hard source of -7.7 vdc at the D24-R25 junction. The primaries of the pulse amplifier output transformers are connected to this point; first-stage transformer primaries are clamped to a point 0.75 vdc more negative.

4.9 6609 PULSE AMPLIFIER

This module contains six 10-mc pulse amplifiers of the basic type. They are driven at E, J, M, R, U, and X; their outputs are available at H-F, L-K, P-N, T-S, W-V, and Z-Y. Type 6609 amplifiers must be driven by the collectors of external pulse inverters. Signals at the bases of these inverters must conform to the specifications set forth in the beginning of this chapter for 6000 series modules. When a signal meets the input requirements, the output is a DEC standard 40-nsec pulse, delayed by 25 nsec and capable of driving 12 units of pulse load.

The module is identical in all other respects to the Type 1609, with the exception of the 1609 feedback circuit. The pulse transformer primaries are returned directly to the -15 vdc supply, rather than to an intermediate supply, and the primary overshoot of the output transformer is lower-clamped directly to -15 vdc.

4.10 6615 ARITHMETIC BUS DRIVER

Four Type 6615 modules are used in the arithmetic processor to gate arithmetic logic and control signals, which arrive at the front connectors, and to generate gated 25-nsec pulses which are fed to buses at the rear to drive the Type 6205 arithmetic register Flip-Flops, AR, MB, MQ, and MI. Each 6615 drives 18 Type 6205 Input Gates in parallel. Jumpering provisions at both input and output permit a variety of logical operations to be performed by this module; in practice, however, input jumpering is the same for all modules, and outputs are jumpered in only two ways. Four 6615 Pulse Amplifiers do not require jumpering at input or output; these implement the AR and MQ shift functions.

The 6615 module uses the basic pulse amplifier. The input transistor is a simple inverter circuit; the common base stage is not required since it is not necessary to mix from inverter collectors--all input pulses are negative. All transformer outputs are terminated with resistors at the 6205 input points.

The base of the carry detection inverter, Q31, is driven through R81 at pin E by a 9-diode negative OR gate whose inputs are tied to the carry outputs of nine AR flip-flops. The presence of a negative carry pulse at any input saturates Q31, resulting in a ground level at output F. Since this terminal is wired in parallel with the corresponding terminals on the other three 6615s, the four load resistors are selected so the value of their parallel combination approximates that of a standard clamped load (1500 ohms). Consequently when all four transistors are cut off, pin F drops to -3 vdc, indicating that the carry function is complete.

4.11 1669 INDICATOR DRIVER

This module contains nine inverters used as transistor switches in indicator lamp circuits. All emitters are grounded; inputs and collector outputs are available at the connector. Operation and

component values are the same as those of the basic inverter described in chapter 1, with one exception: due to the relatively slow circuit operating speed, no capacitors are required across the input resistors. The usual loads are GE 327 bulbs, connected between the collector output pins and -15 vdc. Nominal current output is 30 ma.

4.12 1684 BUS DRIVER

The Type 1684 is a noninverting amplifier used to drive heavily loaded logic lines at speeds up to 5 mc. The module contains four circuits, each comprising two inverters and an output stage that permits the bus to be driven at either logic level by a transistor rather than a clamped load. Inputs are pins K, M, U, and S, each input representing one unit of base load. Outputs at pins L, N, T, and R have a characteristic impedance of 22 ohms and can drive up to five units of base load each. Driving power can be increased to 30 units per output by connecting a 120-ohm resistor between C and E. Resistor coupled outputs at H, J, V, and W increase output impedance when series-driving a bus.

The bus driver circuit, e.g., that with input K and output L, operates as follows: When a ground level is applied to input K, the base of Q1 is held above ground by R2; this holds off Q1, so that its collector is at approximately -4 vdc. R3 then supplies turnon current to the Q2 and Q4 bases through R5 and R4. The Q4 collector is now slightly below ground (provided that output loading does not bring the transistor out of saturation). Since Q3 is cut off by the ground at the Q2 collector, L is at ground with an output impedance of 22 ohms.

When the input level changes to -3 vdc, Q1 saturates, turning off Q2 and Q4. D1 limits reverse bias to the Q2 base and quickly discharges C3. As the Q2 collector falls toward -15 vdc, Q3 turns on and its collector-base diode clamps the Q2 collector to approximately -4 vdc. The emitter of Q3 (for any load that permits the transistor to operate at saturation) is about -3.75 vdc. Because Q4 is cut off, the no-load voltage at output H is therefore -3.75 vdc. Output impedance is still 22 ohms, the value of R9. The -3.75 vdc supply is similar to the -3 vdc supplies of other modules except for an additional series-connected diode. However, unlike standard inverters, all current from negative outputs of this module must pass through R41, the resistor for the supply. Consequently, R41 limits current into negative outputs to approximately 20 ma (5 ma per amplifier). An external 2-watt, 120-ohm resistor can be added in parallel with R41 to increase output current available at -3 vdc to 120 ma.

4.13 4658 I/O BUS TRANSCEIVER

The Type 4658 is designed specifically for the PDP-6 two-way I/O bus system. The four circuits on the module can each drive up to twenty resistor inputs of capacitor-diode gates distributed along a 93-ohm coaxial cable. Access to each amplifier is through a two-element negative OR gate: data inputs are E, K, S, and W; a select level at L is common to all. Levels at these inputs must persist for at

least 2 μ sec. Ground-asserted outputs at F, N, T, and X drive the level inputs of capacitor-diode gates; complements of these coaxial outputs at H, P, U, and Y are used to gate internal registers; outputs J, R, V, and Z usually drive Type 327 28v indicator lamps that are returned to -15 vdc. A ground level asserted at M resets the bus by providing a strong negative level at F, N, T, and X that rapidly discharges the CD gate capacitors. When data is transmitted in the other direction, i.e. when a bus line at F, N, T, or X is grounded externally, pin H, P, U, or Y is asserted negative.

The circuit of Q1 to Q4 is typical of the four amplifiers in the 4658 module. Q1 and Q2--an inverter-and emitter-follower combination--and the negative NAND gate circuit of Q3 have a common output at F. When pin M is at ground, R3 cuts off Q1 by holding its base at ground. With Q1 cut off, its collector is pulled negative toward -15 vdc by R5. This voltage, after current amplification by emitter-follower Q2, appears at F. The Q2 emitter is lower-clamped to -3 vdc, while the Q2 collector potential is stabilized by C2. A negative level at M turns on Q1, resulting in a ground at the Q2 base and therefore at F. D1 to D4 and Q3 form a standard NAND configuration for negative logic levels. When E and L are both negative, R4 pulls the D2-D3 junction negative, turning on Q3 and placing a ground on the bus at F. If either or both gate inputs are positive, Q3 is cut off and the R8-D6 clamped load pulls F down to -3 vdc. Level shifters D3 and D4 ensure good turnoff of Q3.

Inverter Q4 is driven at F, either by the Q1-Q2-Q3 circuit or externally via the I/O bus. When F is at ground, the potential at the D10-R14 junction is approximately -0.75 v. Level shifter diodes D7, D8 and D9 allow R11 to pull the Q4 base positive by about 2.25 v, so Q4 is cut off. The -3 vdc level at the Q4 collector appears at H and J. When F is driven to -3 v, R14 pulls the D9-D10 junction negative until it is clamped by the Q4 emitter-base junction, D7, D8, and D9 to approximately -2.5 v. Since D10 is now cut off, the Q4 turnon current does not flow in the bus, but to the -15 vdc supply through R14. Turning Q4 on results in a ground level at H and J.

4.14 4681 SOLENOID DRIVER

This module contains three driver circuits that operate as switches, transforming DEC standard levels into outputs suitable for driving solenoids. Each driver can control an inductive load, such as a punch solenoid or a typewriter relay, supplying up to 500 ma at operating potentials up to -80 vdc. The switch inputs are K, M, and R; outputs are L, N, and P. Pin E is connected to the external load return voltage source.

A typical circuit operates as follows: When the input at K is -3 vdc, the solenoid driver is quiescent. Since the Q1 emitter is at ground potential, Q1 is saturated and its collector is at ground. The emitter of Q2 is at 2.25 v (the forward voltage drop across D1 to D3). The Q2 base at ground is positive with respect to its emitter, so Q1 is cut off. Under these conditions, the load circuit is open:

no current flows in it and the output is at the load return voltage. When input K is grounded, Q1 cuts off and its collector drops toward -15v , turning on Q2. The load circuit is now completed, allowing current to flow. D4 connects the Q2 collector to the external negative supply, protecting Q2 from the high negative transient that results when the inductive load circuit is opened.

4.15 6684 BUS DRIVER

The 6684 contains four dual-purpose, noninverting bus drivers and associated biasing circuitry. Each driver provides DEC standard levels either to a cable terminated in 100 ohms or directly to a series of base and emitter loads. Circuit delay is approximately 50 nsec.

Each amplifier comprises two series-connected inverter stages driving a push-pull emitter-follower output stage. The load resistor for the second-stage inverter may be clamped to either of two voltages depending upon the output being driven: -3.75 vdc is used for direct driving at H, L, T, and Z; -6.75 vdc is used when driving 93 ohm cables via resistor-coupled outputs at F, N, R, and Y. Each direct output can drive 40 units of base load or four units of dc emitter load at 10 mc; each resistor-coupled output provides DEC standard levels at the cable termination that can drive ten units of base load or one unit of dc emitter load at 10 mc. A 4-digit jumper code specifies the bias used with each amplifier, e.g., 6684-3336.

Consider the circuit of Q1 to Q4 as typical. A -3 vdc level applied to the Q1 base saturates Q1; the resulting ground at the Q1 collector permits R9 to cut off Q2. The Q2 collector is now clamped by T5 and R13 to either -3.75 or -6.75 vdc , depending upon the position of the internal jumper. The negative level is coupled to the common base junction of Q3 and Q4 by R39. Since the amplifier output (the common emitter junction of Q3 and Q4) is referenced to -2.7 vdc by R17 and R25, the emitter-base junction of Q4 is forward biased, while Q3 is cut off. Emitter-follower Q4 therefore conducts current from the load through limiter resistor R3 to the -15 vdc supply; output voltage is either -3 or -6 vdc . When the input level at E returns to ground, Q1 cuts off and Q2 saturates. The ground level at the Q2 collector turns on Q3 and cuts off Q4. Emitter-follower Q3 now conducts current through limiter resistor R29 to the load at H or F, maintaining the output at ground.

CHAPTER 5
DELAYS

The modules described in this chapter provide adjustable delays for standard DEC pulses. Some units make use of delay line techniques to generate comparatively short delay intervals; others use monostable multivibrators to generate wider delay ranges and supply level outputs. The Type 4303 Delay can be extended indefinitely by repetitive triggering.

5.1 1304 DELAY

This module contains input pulse gate Q1, monostable multivibrator Q2-Q3, output level amplifier Q4, and output pulse amplifier Q5. When a DEC 70-nsec pulse grounds input X either directly or through the inverter, level output J switches from its quiescent ground level to $-3v$ for a predetermined interval, then returns to ground. When the level rises at the end of the delay, the circuit generates a pulse at E or F, depending upon pulse polarity desired.

The delay interval is determined primarily by a capacitor connection (three capacitors are available internally, but an external one may be used). Using internal components, the delay may be varied from 0.25 - 500 μ sec in three ranges. With U jumpered to T, potentiometer R5 varies the delay within any range. With no other external connection, C3 provides the minimum range. Other ranges are selected by jumpering H to N or M, thereby adding C4 or C5 into the multivibrator circuit. Delay ranges for these connections are as follows:

None	0.25 - 2.5 usec
H-N	2.5 - 35 usec
H-M	35 - 500 usec

If external delay control is desired, a potentiometer may be connected between S and T. Higher delay ranges may be added by connecting an external capacitor between L and K.

In the quiescent state, Q1, Q3, and Q5 are off; Q2 and Q4 are on. Q1 is held off by a ground at its base or -3 vdc at its emitter. A current of 2.5 ma flows from -3 vdc through D15, R20, the T1 primary and R7 to the -15 vdc supply; 5.5 ma flows from -3 vdc through D2, R21 and R7 to -15 vdc. The resulting 8 ma through R7 maintains the Q1 collector at about $-4v$. Since a steady current flows in the T1 primary, no voltage appears across the secondary. Current flowing from the Q2 base through R3 and the parallel combination R5-R6 (when T is connected to U) holds Q2 on.

When a pulse at X or Y triggers the 1304 Delay, the resulting 4v drop across the T1 primary is coupled to its secondary winding. Terminal 4 now goes negative as current through the primary increases linearly to 10 ma from its quiescent value of 2.5 ma. During this increase the voltage across

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the primary at first remains nearly constant due to the clamping action of D2 and R21. When the T1 primary draws more than 8 ma, however, D2 is back biased, and R21 is removed from the primary circuit. As the primary circuit resistance is thus increased, the primary voltage decreases more rapidly.

D1 couples the negative pulse at T1-4 to the Q3 base; Q3 then turns on and its collector rises to ground. The low forward resistance of D7 and R11 shunts the T2 primary so no current flows in the secondary. The junction of D4 and R12 now rises to ground, turning off Q4. The output level at J then drops to -3v, indicating the start of the delay interval. The ground at the Q3 collector is applied through D5 to pin H where it is coupled to the Q2 base by C3, C4, or C5 (depending upon the connection made to H). Q2 now cuts off and its collector drops to -3v. R4 then draws base current from Q3, holding on Q3 even after the pulse at T1-4 ends.

The monostable multivibrator remains in this state, Q2 off and Q3 on, for the time interval required to charge the capacitance in the Q2 base circuit. The RC time constant, which determines this interval, depends upon the capacitors in use, and the resistance of R3 in series with the parallel combination R5-R6. When the time delay capacitors have charged to a sufficiently negative voltage, Q2 turns on. The rise in its collector voltage is coupled through R4 and C6 to the Q3 base: Q3 then cuts off, causing the T2 primary current to fall to its quiescent level. The resulting negative pulse in the T2 secondary is applied to the Q5 base, turning it on. The pulse amplifier comprising Q5 and T3 generates a DEC standard 70-nsec pulse across outputs E and F. C8 flattens the output pulse top. When the T2 secondary voltage drops to 0, Q5 turns off and the output pulse ends. As Q3 turns off, the junction of D4 and R12 returns to -3v, turning on Q4. Level output J therefore returns to ground, indicating the end of the delay.

5.2 4301 DELAY

Except for delay ranges and pulse widths, this module is identical to the Type 1304 Delay. Five internal capacitors enable delaying 0.4-usec input pulses by 2.5 usec to 200 msec in five ranges. Potentiometer R7 can be used to vary the delay within any range by jumpering U to T. With no other external connections, C4 provides the minimum range. Other ranges are selected by jumpering H to N, M, P, or R, thereby adding one of C5 to C8 into the multivibrator circuit. C4 provides a delay of 2.5 - 25 usec. The additional values of capacitance (C5 to C8) increase the range by successive factors of approximately 10. Circuit recovery time is 20% of the maximum delay in the selected range. If external fine control of the delay interval is desired, a potentiometer may be connected between S and T. Larger delay ranges can be achieved by connecting an external capacitor between L and K. All 4301 input and output pins, with the exception of two additional delay capacitor connections at P and R, are identical to those of the Type 1304.

5.3 4303 INTEGRATING DELAY

This module contains two monostable multivibrators, two difference amplifiers (slicers), three inverters, a positive capacitor-diode gate, and a negative dc supply. The 4303 circuit has flip-flop-type logic level outputs: in the 1 state, the 1 output is at -3 vdc, the 0 output is at ground; in the 0 state, output polarities are reversed. When any of three inputs is pulsed, the circuit assumes the 1 state; it returns to the 0 state after a selected delay, which begins with the termination of the input signal.

The multivibrators are Q2-Q3 and Q10-Q11; the slicers are Q5-Q6 and Q7-Q8. The inverters are Q1, Q4, and Q9; the capacitor-diode gate is C1-R1-D1. Voltage levels of -0.75 , -1.5 , -3 , -4.5 , -5.25 , and -6 vdc are tapped from the internal negative supply at the cathodes of D16, D15, D13, D11, D10, and D9. Three inputs are provided at pins K, S, and R. The K input may be either a DEC standard $0.4\text{-}\mu\text{sec}$ negative pulse or a negative level. The S input may be either a DEC standard $0.4\text{-}\mu\text{sec}$ positive pulse or a positive-going level change; this pulse is gated to the Q2 base by a ground at T. Input R requires a positive pulse such as the output of a positive capacitor-diode gate similar to C1-R1-D1. The 1 and 0 outputs are W and U.

The delay is variable from $3.4\ \mu\text{sec}$ to 0.9 sec in five overlapping ranges. Connection of one of five internal capacitors determines the delay range. C7 is permanently connected and gives the shortest range. Connecting C6, C8, C9, or C10 (E, F, H, or J) to ground (D) increases the range by successive factors of approximately 10. Potentiometer R10 determines the delay within each range if Y is jumpered to X. Alternatively, an external potentiometer connected between Z and X may control fine delay.

In the quiescent state, Q1, Q3, Q4, Q5, Q8, Q9, and Q10 are off; Q2, Q6, Q7, and Q11 are on. Voltage divider R2-R3 shifts the ground level at input K positive, biasing Q1 off. Multivibrator Q2-Q3 is in its stable state, with Q2 held on by base current flowing through R5, and Q3 held off by voltage divider R8-R9. With the Q2 collector at ground, voltage divider R11-R12 biases Q4 off.

In the first slicer, Q5 is off and Q6 is conducting. D6 clamps the Q6 collector at -0.75v , holding Q6 out of saturation. The common-emitter connection of npn transistors Q5 and Q6 follows the voltage (-1.5v) at the base of Q6. Consequently Q5 is cut off. The other slicer transistors, Q7 and Q8 are on and off, respectively. The series combination of R13, R14, and potentiometer R10 draws sufficient current from the Q7 base to saturate that transistor, even if the potentiometer is set at maximum resistance. The saturation of Q7 holds the common emitter connection of Q7 and Q8 at -5.25v , the Q7 collector voltage. The more positive voltage (-4.5v) at the Q8 base holds it at cutoff. Q9 is therefore back biased through R19 and is also cut off. The voltage divider made up of R23 and the parallel combination R21-R24 holds Q10 off. Consequently, multivibrator Q10-Q11 is in its stable state, with Q10 off and Q11 on.

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The circuit is triggered from the quiescent state when an appropriate input at K, R, or S drives the Q2 base positive. Multivibrator Q2-Q3 flips to the temporary state with Q2 off and Q3 on. Diode D4 clamps the Q2 collector to $-3v$. R11 and C5 couple this $-3v$ level to the Q4 base, saturating it. The grounded collector of Q4 drives the bases of Q5 and Q7 positive. Q7 drives output multivibrator Q10-Q11 to its temporary state; Q5 forms part of the feedback loop that returns the signal to input multivibrator Q2-Q3, causing it to revert to its stable state.

As the Q7 base goes positive, Q7 turns off and Q8 turns on, so their common emitter connection rises to the Q8 base voltage. Q8 does not saturate because its rising collector voltage is clamped at $-5.25v$ by the Q9 turnon. (Q9 does saturate and its collector drops to $-5.25v$). R20 couples the Q9 collector voltage to the Q10 base, turning it on. Multivibrator Q10-Q11 flips to the temporary state, with Q10 on and Q11 off. The output is now in the 1 state (W at $-3v$, U at ground).

In the feedback loop to input multivibrator Q2-Q3, R14 drives C7 (and any other capacitor that may be in parallel with it) toward ground. When this voltage reaches approximately $-1.5v$, Q5 saturates heavily, forward biasing both its base-emitter and base-collector junctions. The larger part of the Q5 base current flows to its collector, which is consequently more negative than its emitter. Q6 is thus cut off. The Q6 collector goes positive, forward biasing D5 and cutting off Q3. Q2 now turns on (provided it is not held off by a continuing positive level at R). This grounds the Q4 base, cutting off Q4 and initiating the discharge of the timing capacitors. Before the Q7 collector can return to its quiescent state, C7 (and any additional capacitor in parallel with it) must discharge through R13 and potentiometer R10. As C7 begins to discharge, Q5 turns off and Q6 turns on. D5 becomes back biased, disconnecting R16 and R17 from the Q3 base circuit. From this time on, even though the full delay interval is not yet over, the circuit can be retriggered by a positive pulse at S, or a negative input at K.

When the Q7 base becomes more negative than $-5.4v$, Q7 turns on, and Q8 turns off. The $-6v$ supply back biases Q9 via R19, turning it off. The rise in voltage at the Q9 collector cuts off Q10, returning the output multivibrator to its stable state. The output returns to the 0 state (W at ground, U at $-3v$), indicating the end of the delay.

If the Q1 input is held at $-3v$ d.c., C7 charges up to $-1.5v$ and stays there, and the output remains in the 1 state. Return to the 0 state occurs a fixed interval after the removal of the negative Q1 input. When input pulses arrive at shorter intervals than the delay period, the output similarly remains in the 1 state, returning to the 0 state a fixed interval after the last pulse.

5.4 DELAY LINES

These modules contain one or more delay lines that provide relatively short delays for standard negative pulses, although the circuits can also be used to delay level transitions. With each line is an inverter driven by the delay line output; the collector, often the emitter, and occasionally the base of the inverter are available at the external connector. To simplify coaxial or twisted-pair connections, individual ground return pins are adjacent to all collector outputs. Every line has taps so that various delays can be selected up to the total length of the line. Modules in which the taps are available at the external connector contain one or two lines; those in which delays are selected by internal jumpers contain six. The jumper code is six digits which correspond left to right to the alphabetical order of the output pins. A 1 in a given digit indicates the shortest nonzero delay on the corresponding line, a 2 indicates the next longer delay, and so forth. The delay configuration and the pin connections or jumpers for selection in each module are shown in the circuit schematics. In every case, the delay across the output inverter must be added to the delay selected: 20 nsec in the 1000 series modules; 12 nsec in the 6000 series.

For the operation of a typical delay line, consider the Type 1310. A negative pulse at input X causes a ground pulse after a predetermined delay at inverter output E. A clamped load connected to E (or some electrically equivalent point) holds it negative while the inverter is off. When the circuit is quiescent, R1 furnishes current to hold Q1 off. Terminating resistors R2 and R3 prevent signal reflections from the ends of the delay line. R4 and R5 are used as attenuators when selecting a shorter delay, to match the attenuation of a signal traversing a greater line length. D1 isolates the input from reflections caused by mismatch at the output tap.

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CHAPTER 6 PULSE CIRCUITS

The PDP-6 uses four pulse circuits, Pulse Generators 1410 and 4410, and Clocks 4401 and 4407. A pulse generator is similar to a pulse amplifier, since it produces a DEC standard pulse whenever its input is triggered, but it differs in that it can be triggered by slow, irregular voltage changes such as those produced by mechanical switching. The clocks generate trains of 0.4- μ sec pulses: the 4401 frequency is adjustable, but the 4407 frequency is predetermined by the crystal oscillator it contains.

6.1 1410, 4410 PULSE GENERATORS

These two pulse generators have identical circuits and pin connections; they differ only in output pulse width: the 1410 output is a DEC standard 70-nsec pulse; the 4410 output is a DEC standard 0.4- μ sec pulse. The following description uses the component designations for the 1410.

The module contains a Schmitt trigger circuit (Q1-Q2), an output pulse amplifier (Q5), and an RC filter (R1-R2-C1). It generates an output pulse whenever its input drops from a value more positive than -1.0v to a value more negative than -2.0v. If no filtering is required, the input is applied to S. However, if the internal filter is needed (e.g., when the circuit is used in conjunction with a mechanical switch), S and U are jumpered and the input applied to Z; the negative trigger input to Z is then obtained by mechanically switching K to Z. The combination of capacitor filtering and the hysteresis of the Schmitt circuit prevents the switch contacts from generating more than one pulse per closure. The output terminals are E and F; the output pulse is negative at E when F is grounded, positive at F when E is grounded.

For an initial ground input at S or Z, Q1 is off and Q2 is on. The Q2 emitter follower action holds the Q1 and Q2 emitters to about -1.8v. Divider R5-R6-R9-R10 determines Q2 base voltage. D2 isolates Q1 and Q2 emitters from the -1.0v level at the R12-R13 junction. The Q2 collector is quiescently at -4v. The current through the T1 primary is held steady at about 10 ma, and no voltage appears across the secondary. The Q5 base is therefore held at ground through the T1 secondary so that Q5 is cut off, with its collector at approximately -7.5v.

The circuit is triggered by a negative voltage applied to its input. Q1 begins conduction when its base becomes more negative than its emitter; i.e. when the input falls below -2.0v. As Q1 conducts, its collector voltage rises toward ground. R6 and C2 couple the rising Q1 collector voltage to the Q2 base, thereby cutting off Q2. This pulls the common emitter connection of Q1 and Q2 more positive, speeding the Q1 turnon by positive feedback. This method assures a fast change of state, independent of the fall time of the input signal. The T1 field collapses with the turnoff of Q2, inducing a negative pulse

at T1-4. The pulse turns on Q5, whose collector rises rapidly to ground, causing a pulse to appear across the T2 secondary, pins E and F. C4 flattens the pulse top by maintaining a more constant rate of change of current in the T2 primary over the pulse period.

When the Q1 base input again rises toward ground, the Q1 emitter follows until its base is at approximately $-1v$. At this point, D3 is forward-biased and clamps the emitter voltage. Further input voltage rise cuts off Q1; the resulting drop at the collector is coupled through R6 and C2 to the Q2 base, turning Q2 back on and returning the trigger circuit to its initial state. Current is now reestablished through the T1 primary; the resulting positive pulse at T1-4 only drives Q3 further into cutoff and the output pulse amplifier is unaffected. D1 and R11 prevent ringing in T1.

6.2 4401 CLOCK

This module comprises an astable multivibrator (Q1-Q2), a pulse amplifier-shaper (Q3), and an output pulse amplifier (Q4). The Type 4401 generates DEC standard $0.4\text{-}\mu\text{sec}$ pulses at E or F at any frequency from 5 cps to 500 kc. The interval is divided into five overlapping ranges; within each range, the output frequency is continuously adjustable. The output pulse train is inhibited by applying -3 vdc to a disconnect diode whose anode is connected to V.

The frequency range is determined by the amount of capacitance between T and V; one of five capacitors may be selected by an external jumper. Connecting T to M selects the range of 5-50 cps; connecting T to R, P, N, or U increases the range by successive factors of 10. Connecting an external capacitor between V and T will extend multivibrator frequency range. Potentiometer R4 adjusts frequency within the selected range when X and Y are jumpered. An external fine control potentiometer can be connected between Y and Z.

Diodes D1 to D6 determine multivibrator operating voltages: a tap at the D3-D4 junction holds the Q1 base at -2.25 vdc ; -3 vdc for the Q1 and Q2 collector supply is provided at the D4-D6 junction. Since R4 varies the Q1 operating point over a wide range, a dual collector load is provided for Q1. R3 is principal load for low operating current; at higher currents, D5 conducts and the load is shared by R2.

Q1 and Q2 commute at a rate that is a function of the RC time constant of the range-determining capacitor (one of C3 to C7) and the series combination of R1 and R4. An output pulse is generated during each cycle of the multivibrator at the Q2 turnoff. Assume that Q1 is turning off and Q2 is turning on. The Q2 emitter voltage follows the negative-going voltage at the Q1 collector. C3 (if T is jumpered to M) couples the negative transient to the Q1 emitter. This feedback rapidly triggers the multivibrator to its first state, Q1 off and Q2 on. The T1 secondary now generates a positive pulse at the Q3 base, which serves only to drive Q3 further into cutoff; the output pulse amplifier is therefore not affected.

The multivibrator remains in this state while C3 charges through R4, R1, Q2, and the T1 primary, pulling the Q1 emitter toward ground. When the emitter voltage becomes more positive than $-2.25v$ (the

Q1 base potential), the transistor turns on and Q1 collector-emitter feedback triggers the multivibrator to its second state, Q1 on and Q2 off. Note that if V is held at -3 vdc, Q1 cannot turn on. The turnoff of primary current in T1 generates a negative pulse at T1-3. This pulse saturates Q3, grounding T2-2 and turning on Q4 with a negative pulse at the base. The output pulse amplifier (Q4, T2, T3) generates a DEC standard $0.4\text{-}\mu\text{sec}$ pulse across E and F. This pulse is positive at F if E is grounded, negative at E if F is grounded. C8 flattens the output pulse top by maintaining a high rate of change of T3 primary current for a longer time. The T3 primary overshoot is damped through R8 and D7.

The multivibrator remains in the second state while C3 discharges through R5, Q1, and the Q1 collector load. When the discharge current decreases to about 6 ma, the Q2 emitter becomes more positive than its base, so Q2 begins to turn on, turning off Q1 and starting a new cycle.

6.3 4407 CRYSTAL CLOCK

This module contains a crystal oscillator (Q1-Q2-Q3), an oscillator output amplifier (Q4), a Schmitt trigger (Q5-Q6), and an output pulse amplifier (Q7). It generates DEC standard $0.4\text{-}\mu\text{sec}$ pulses, either positive or negative, at a frequency determined by the oscillator crystal. This frequency may be between $5\text{-}500$ kc: in the PDP-6 Teletype interface the crystal is series resonant at 14.08 kc. Negative pulses are obtained at E or positive pulses at F; the unused pin must be grounded.

Positive feedback from the collector to the emitter of Q1 sustains oscillations at the resonant frequency. This feedback is obtained through the common emitter junction of Q1 and Q3. Since the impedance of the crystal is minimum at resonance, positive feedback is maximum at this frequency. The parallel resonant circuit C1-C2-L1 helps to stabilize the gain of Q1 and makes it possible to tune the oscillator through a narrow band about the crystal resonant frequency. Zener diodes D1 and D2 isolate the oscillator from supply variations. Q3 collector output is applied through Q4 to the Schmitt circuit, Q5-Q6, which converts the oscillator output to a square wave.

Assume Q5 off and Q6 on. Q6 emitter follower action holds their emitters at approximately -1.8 v. Divider R11-R13-R14-R16 determines the Q6 base voltage. Diode D5 isolates the emitters of Q5 and Q6 from the -1.0 v level at the junction of R17 and R18. The Q6 collector rests at -4 v. Current through the T1 primary is held steady at about 10 ma, and no voltage appears across the secondary. The T1 secondary holds the Q7 base at ground, so Q7 is cut off. The Q7 collector is, therefore, at approximately -7.5 v, with the T2 secondary quiescent.

The Schmitt circuit is triggered when the Q5 base falls below -2 v. R13 and C4 couple the rising collector voltage of Q5 to Q6, cutting it off and pulling up the common emitter connection of Q5 and Q6. This positive feedback ensures a fast change of state, independent of input signal fall time.

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As Q6 turns off, the T1 field collapses, inducing a negative pulse at T1-3. This negative pulse is amplified by Q7 and appears across the T2 primary, and hence across E and F. The pulse amplifier shapes the output to 2.5v amplitude and 0.4- μ sec duration. C7 flattens the pulse.

When the Q5 base input rises toward ground, the emitter follows until it reaches approximately -1v. At this point D5 again conducts, clamping the emitter voltage. Q5 cuts off as its base rises above -1v. The resulting negative transition at the Q5 collector turns Q6 back on, returning the trigger to its initial state. Current flow is thereby reestablished through the T1 primary, resulting in an induced positive pulse at T1-3. This positive pulse, however, drives Q7 only further into cutoff, so the output pulse amplifier is unaffected. D4-R15 and D6-R20 prevent ringing in the transformer primaries.

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CHAPTER 7 POWER CIRCUITS

The PDP-6 power supplies convert standard 110 vac to dc power. They include the Types 728 and 778 which supply the +10 and -15v required by the logic, and the Type 734 whose output, variable from 0 - 20v, may be used for marginal checking. A power control governs line voltage to the power supplies and to motors in peripheral equipment. The particular control used in any situation depends upon the requirements of the system; some units provide two-step control, some provide additional control functions. One control, Type 823, allows the logic to govern operation of the punch motor and is mounted directly on the motor. All other power supplies and controls are mounted on the rear plenum door of a standard DEC equipment bay, although in the arithmetic processor, the 734 Supply is mounted behind the console in/out indicator panel.

7.1 728 POWER SUPPLY

This unit supplies the power required by most of the PDP-6 modules. Outputs are +10vdc at 0 - 7.5 amp and -15 vdc at 1 - 8.5 amp. When both outputs are used concurrently, the available current is limited as follows: -10 vdc, between 0 and 7.0 amp, -15 vdc, between 1 and 8.0 amp; and combined, by the relationship

$$5i_{+10} + 6i_{-15} = 53,$$

where i is current supplied.

The +10 output is regulated to between +9.5 and +11v, the -15 output, between -14.5 and -16v. This regulation holds for minimum to maximum load in the presence of line variations from 105 to 125 vac. Output ripple is less than 350 mv.

T1 steps down the line voltage to 10-0-10 vac and 15-0-15 vac. D2 and D3 are connected to the 10v secondary taps as a positive full-wave rectifier. C2 and C4 filter out the ac component of the output. R1, in parallel with the 10v load, maintains the output within regulation tolerances even when no current is drawn externally. D1 and D4 are connected to the 15v secondary taps as a negative full-wave rectifier. C1, C3, C5, and C6 are filters.

The design simplicity of the Type 728 is made possible by the fact that the saturated-core resonant transformer (T1) incorporates inherent overload protection. Even with shorted outputs, only a limited current can be drawn. This self-limiting feature obviates series impedance elements at the filter inputs. Thus the dc output impedance is kept low, rendering regulating devices unnecessary.

7.2 734 VARIABLE POWER SUPPLY

This unit furnishes dc power for marginal checking of the PDP-6 modules. For a nominal 110 vac input, output voltage is continuously variable from 0 - 20 vdc (no load). Maximum output voltage drops 3v at full rated load of 2.5 amp.

Line power at 110 vac is stepped down by transformer T1 (only half of the secondary is used), which drives an M5 Variac. By adjusting the position of the Variac tap, any voltage within the range of 0 - 20 vac is available (clockwise rotation increases voltage). The Variac output is applied to a bridge rectifier, whose diodes are oriented so that the dc output at the D2-D4 junction is positive with respect to the D1-D3 junction. Parallel capacitor C1 filters the output; R1 improves voltage regulation for small load currents. A slow-blow 5-amp fuse at the positive output protects the supply against overload. The output voltage is indicated on a 0-30 vdc meter.

7.3 778 POWER SUPPLY

The Type 778 is a dual floating 15 vdc power supply, capable of supplying 8.5 amp from each channel. The two supplies each contain a transformer, a full-wave silicon rectifier, and three filter capacitors.

In each unit, a resonant transformer steps down the line voltage to 15-0-15 vac. The diodes are connected as negative full-wave rectifiers. The simple design of this supply is made possible by use of saturated-core resonant transformers that provide inherent overload protection; even with shorted outputs only a limited current can be drawn. This self-limiting feature obviates series impedance elements at the filter inputs. Thus the dc output impedance is kept low, making regulating devices unnecessary.

The outputs remain between -14.5 and -16v over variations in load from minimum to maximum and in line voltage from 105 - 125v. Maximum peak-to-peak ripple is 1.0v; required line frequency regulation is 60 ± 0.5 cps.

7.4 811 POWER CONTROL

This unit controls power turnon and turnoff in various peripheral devices. An 811 in the arithmetic processor supplies line voltage to the reader, punch, and keyboard-printer whenever computer power is on (the power control output to the punch is actually applied to the 823 SCR Power Control).

As long as the circuit breaker is closed, K1 applies line power to the control output through contacts A and B. The unit includes a two-position switch to allow a choice of local/remote control and two additional relays K2 and K3 to provide a means of control by remote signals. All relay contacts are normally open. The K1 coil is energized by 115 vac, K2 and K3 by -15 vdc. Wiring connections for each application are made at the 10-terminal Jones strip, and a diagram of the configuration is included in the appropriate system maintenance manual.

As an example of a typical application, consider the situation in which terminal 3 is connected to 8, 6 to 7, and 7 to 1. Then the position of the switch that connects 1 to 3 provides for local power turnon by energizing K1 either directly if 7 is wired to 9, or by means of an external power switch if 7 is connected to 9 through such a switch. With no connection to terminal 2, the other switch position provides for remote turnon so that -15v applied to 5 energizes K2 bypassing the switch. Relay K3 allows delayed turnoff if desired. At turnon, the -15 vdc remote signal charges C1 through D4; at turnoff, C1 energizes K3 momentarily, delaying the K1 release.

7.5 823 SCR POWER CONTROL

The Type 823 is an ac power control capable of high speed response to low power logic signal inputs. The controlling element is a high speed reed relay designed to form the collector load for any standard DEC pnp stage among the 4000-series inverter and diode modules. The relay in turn triggers a silicon controlled rectifier which accomplishes the primary power switching function.

The silicon controlled rectifier is a four-layer pnp device that behaves much like a gas thyatron. At reverse-bias voltages below the avalanche value, the SCR blocks the flow of current. Under forward-bias conditions the SCR also blocks current flow, but it can be switched into a high-conduction state by a small positive current from gate to cathode. The SCR can thus control very large amounts of power in response to a low power signal. Once it is in the high-conduction state, it continues to conduct indefinitely, even after removal of the gate signal, until the anode current is interrupted or diverted. It then regains its forward-bias current blocking capability.

In the Type 823, the SCR works in conjunction with a 4-diode bridge, which is in series with the punch motor across the power line. One side of the 115-vac 60-cycle power line is connected to AC IN. Under control of the SCR, power flows through the bridge to AC OUT, through the punch motor, and back to the ac line. Shown at the left is K1, the low power reed relay that operates from a logic level input to control the trigger input to the SCR gate.

Assume initially that the SCR is blocking forward current flow. R2 holds the gate close to cathode potential. When the logic provides ground level at INPUT, K1 energizes and its contacts allow positive gate current to flow through R1 into the SCR gate, to trigger the high-conduction state. During positive half-cycles across the power line, current flows from AC IN through D2, the SCR, D3, and the motor back to the line. During negative half-cycles current flows through the motor and returns to the line through D1, the SCR, and D4. When the logic releases the ground level at INPUT, K1 removes the gate current through R1, and the SCR reverts to its forward current blocking condition when the instantaneous line voltage swings through zero.

7.6 829 TWO-STEP POWER CONTROL

This unit is used in situations that require a two-step application of power such as in a core memory, where core drive circuits must not receive power until after the logic does but must be turned off first. The 829 is used in the Type 161 Core Memory and in some arithmetic processors. Wiring connections for use with the memory are shown in the memory control drawings, for use with the processor in the console drawing.

The left secondary of the transformer shown at the left supplies a 60-cycle signal which may be applied to a pulse generator for use as a real-time clock. The other secondary drives a diode bridge that supplies unregulated filtered 15 vdc for the relays. Line power applied to the control input is coupled to the outputs through contacts 2 and 3 of K3 and K4. K1, a fast on/slow release relay, picks up K3, which couples the input to the upper output. K2, a slow on/fast release relay, energizes K4 to provide power at the lower output.

If TP7 is connected to TP8, turning S1 to local energizes K5, which in turn energizes both K1 and K2. Through the upper contact sets, K1 energizes K3 immediately, K2 energizes K4 after a delay of 3 - 5 sec. The lower contact sets provide the same type of operation for any desired external switching function. For example, if TP17 or TP20 is connected to signal ground (at the logic), TP16 and TP19 remain at ground for several seconds after turnon to enable a power clear function. When S1 is turned off, K2 drops out immediately but K1 holds K3 on for several seconds.

If S1 is in remote, the power control can be turned on by an external switch connected across any of the TP pairs 1-2, 3-4, or 5-6. Of course remote turnon can also be accomplished by applying an external -15v to TP1, 3 or 5, directly to TP7, bypassing the local/remote switch.

7.7 832 TWO-STEP POWER CONTROL

This unit is used in situations that require a two-step application of power such as in a core memory, where core driving circuits must not receive power until after the logic but must be turned off first. K3 connects line power to the upper output, K2 to the lower output. All three relays operate on 115 vac. Energizing K1, a fast on/slow release relay, in turn energizes K3. If power is desired at the delay on/fast off output, closing S2 allows K2 to be energized whenever K1 is energized. For typical use terminal 1 is connected to 3, and 5 to 6. Then turning S1 to local picks up K1, and picks up K2 through S2. Line voltage appears immediately at the upper output, but, since K2 operates slowly, there is a 3 - 5 sec delay before power appears at the lower output. When S1 is turned off, the lower output goes off immediately but the upper output is delayed. For remote control, S1 is turned to remote and the power control is turned on and off by an external switch connected across terminals 1 and 2.

7.8 834, 835 ONE-STEP POWER CONTROLS

These units provide single-step power application by means of a remote switch closure. The 835 is the main power control for the arithmetic processor, and the wiring connections for that application are shown at the upper right in the console drawing. The two power controls are identical except that the 835 contains a filament transformer whose 60-cycle output drives a pulse generator to provide a real-time clock.

For standard applications terminal 1 is connected to 3, and 5 to 6. Turning S1 to local energizes K1, whose contacts couple the line voltage from the control input to the output. For remote control S1 is turned to remote and K1 is then controlled by an external switch connected across terminals 1 and 2.

PDP-6 CIRCUITS

CHAPTER 8 MODULE REPAIR

All DEC modules are exhaustively checked for faulty or marginal operation, both prior to their incorporation into the computer and during operation as a functional part of the system, to make malfunctions due to defects of workmanship or components as unlikely as possible. But module failures sometimes do occur, however seldom, and some provision must be made to restore them to proper operation. After locating a faulty module, the user may choose from two courses of action: he may return the module to DEC or attempt to repair it himself.

DEC recommends return of all defective modules since the facilities available at the plant ensure that all possible causes of failure can be investigated and eliminated. However, if there are appropriate test facilities in the field, well-staffed with engineering and test personnel competent in computer maintenance, the user may wish to try his hand. This chapter is a guide to module repair in the field. Replacement components may be obtained either directly from DEC or commercially. Equivalency charts on the schematics show the JEDEC numbers corresponding to DEC part numbers. Almost all non-inductive components except distributed-constant delays are available through local electronic part distributors.

8.1 TOOLS AND TEST EQUIPMENT

In addition to standard shop tools, including a 6v soldering iron with isolation transformer, the following are recommended:

Multimeter	Simpson model 260A, Triplet Model 630NA, or equivalent
Subminiature alligator clips	Mueller Type 30 or equivalent
Oscilloscope	Tektronix Type 581 (50 mc) with Type 82 dual-trace vertical pre-amp, or equivalent
Long-lead probes	Tektronix P-6002 or equivalent
Current probe	Tektronix P-6016 or equivalent
Module puller	DEC Type 1960 (supplied without charge)
Module extender	DEC Type 1954 (supplied without charge)
Pigtail module extender	Modified DEC Type 1954 (below)

In complex installations or in multiple installations, an independent bench module tester may be desirable. A tester for DEC plug-in modules can be made up from a Type 722 Power Supply, a

commercial variable signal generator (10 mc maximum), standard DEC signal-generating modules (e.g., Pulse Generator 1410, Variable Clock 6401) and suitable switching circuits. A desirable addition to the tester is a 734 Power Supply, which permits marginal checking of plug-in units at the bench.

A pigtail module extender can readily be fabricated from a standard DEC Type 1954 Extender. Disconnect the small wire leads to terminals A, B, and C of the extender, and solder 8-foot leads to the three terminals. Solder alligator clips to the free ends of the leads. This permits convenient marginal testing of an individual module while it is in place (through the extender) without disturbing the remainder at the mounting panel.

8.2 REMOVAL AND REPLACEMENT

It is advisable to turn off system power before extracting or inserting a module. Modules can be removed conveniently with the DEC Type 1960 Module Puller. Carefully hook the small flange of the puller over the center of the module rim and gently pull the unit out of the mounting panel. Use a straight, even pull to avoid damaging the plug connections or twisting the etched circuit. Since the puller does not fasten to the module, prevent it from falling by holding the rim in one hand as you pull it from the mounting panel.

When replacing a module, always position it so that the component side of the board is to the right and the printed wiring to the left. The aluminum rim extends along the bottom edge beyond the plug. When a module is properly installed, this extension fits into a matching slot in the mounting panel. Should the module be upside down, the extension prevents it from making contact with the mounting panel socket. Carefully slide the module between the guide ridges embossed on the mounting panel surfaces until the plug makes contact. If plug and socket are properly aligned, gentle pressure is sufficient for full insertion. Do not force the connection if plug and socket are not aligned. Occasionally, slight movement of the module within the guide ridges may be necessary to match the plug with its connector.

The tape reader printed circuit cards (mounted on top of the reader chassis) are removed by grasping the top of the card with the thumb and index finger of one hand and the edges of the card with the thumb and fingers of the other hand. A gentle pull disengages the card from its socket. The card then slides straight up and out of the mounting panel. A card is inserted by guiding it into the two panel slots and allowing it to slide downward until it contacts the socket. A slight downward push fully engages the connections. Component sides of these cards are to the right when observed from the reader front.

Connections to power supplies and controls are made both by wiring at barrier terminal strips and by cables terminating in plugs. Although the barrier strip wiring is color coded, these markings may be absent from the chassis of the power unit. Before removing or replacing a power unit, clearly mark all unlabeled connections both on the unit to be removed and on the spare to be installed. After disconnecting the unit, release it by removing the Phillips-head mounting screws on both sides.

A large number of DEC modules are equipped with jumpers to increase their versatility in performing logic functions. Nomenclature for such a module on the logic diagrams includes a code defining jumper locations for that module in the given mounting panel position. The codes differ among module types and are noted in the circuit descriptions. Spare modules are supplied with all jumpers in place, indicated usually by an R. Before replacing a module remove all jumpers on the spare except those required and mark the spare with the correct code.

8.3 MODULE TROUBLESHOOTING

Malfunctions within a single module may be located in two ways. The first, in situ or active circuit troubleshooting, involves use of the module extender, the pigtail extender, the oscilloscope, and small two or three-instruction exercise loops like those described in chapter 9 of the arithmetic processor manual.

The second method is bench troubleshooting, involving use of a suitable multimeter, the DEC equipment listed in section 8.1, an oscilloscope, and standard bench test equipment such as an in-circuit transistor and diode checker, a regulated bench power supply, etc. A bench tester may be built up from DEC modules to provide active-circuit troubleshooting (signal tracing) independently of the computer. Information on system design with DEC modules, helpful in assembly of a bench tester, is in the Digital Modules Catalog (A-705A) available from DEC without charge.

8.3.1 In-system Troubleshooting

The extender permits troubleshooting of many modules while the system is operating. There are, however, exceptions to use of the extender: the high operating speed of the 6000-series modules may not allow them to function properly on the extender, due to the added inductive coupling of the extender leads. Moreover, no extender is provided for double- and triple-size modules; if these cannot be repaired at the bench, return them to DEC. To use the extender turn off system power, remove the module and insert the extender in its place, plug the module into the exposed end of the extender and finally, turn the power back on. To apply marginal voltages to an individual module, use the pigtail extender instead, and furnish pins A, B, and C with appropriate marginal check voltages via the three clipleads.

Active troubleshooting can often be simplified if knowledge of PDP-6 logic enables the user to exercise the questionable module with the computer. A repeat switch and speed control on the console allow repetition of the key functions with a delay adjustable from 8 sec down to 3.4 μ sec.

CAUTION

Although DEC circuits are designed with internal safeguards which prevent damage from opening or shorting the output terminals on a single unit, they are not proof against all accidental shorts which might be produced while testing the unit on an extender. Care must also be exercised when testing terminals on the wiring side of the racks.

8.3.2 Bench Troubleshooting

If a simple inspection fails to reveal the cause of the trouble, multimeter resistance readings can often isolate it. Resistance readings allow a rough check on emitter-base diodes of transistors (it is essential to determine the internal battery polarity of the multimeter; this polarity is sometimes opposite to the normal polarity of the leads). Note that although incorrect resistance readings are a sure indication that the transistor is defective, correct readings give no guarantee that the transistor is good; it may have other troubles. Several inexpensive in-circuit transistor and diode checkers are available commercially--those generally provide a more reliable indication of diode or transistor quality.

Damaged or cold-soldered connections can also be located with a multimeter. Set the multimeter to the lowest resistance range and connect it across the suspect junction. Poke at wires and components around the connection with a probe or hand. Often the response time of the multimeter is too slow to detect rapid transients produced by intermittent connections. Current interruptions of very short duration can be detected by placing a 1.5v battery, in series with a 1.5K resistor, across a connection and observing the voltage across the resistor with an oscilloscope.

Use a 6v soldering iron with an isolation transformer to remove or replace defective components. Avoid excessive heat which can cause damage to components and might even delaminate the etched wiring. Semiconductors require special care--wherever possible, attach a copper alligator clip or other heat sink to the lead being soldered, to reduce the amount of heat transferred to the component.

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